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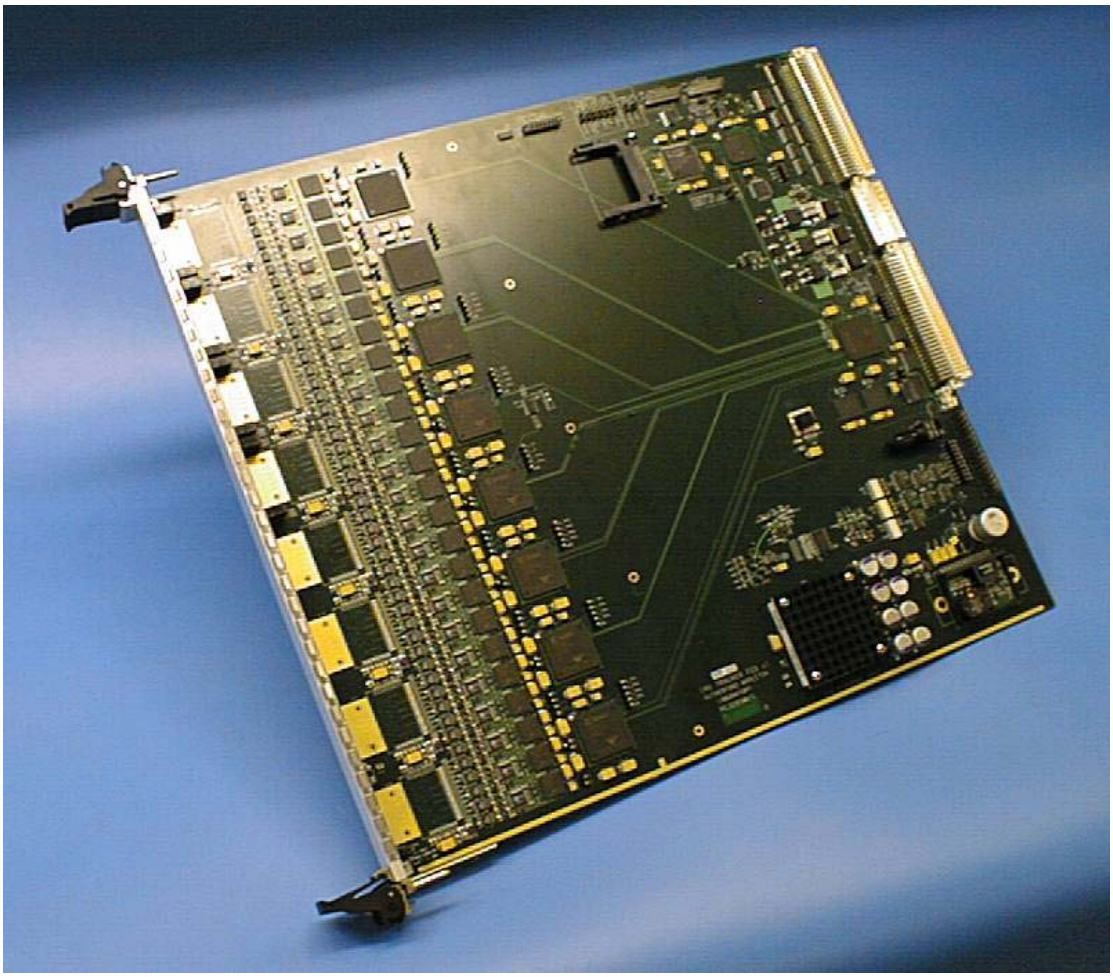
Introduction

General Description

The Front End Driver (FED) is a 9U 400mm VME64x card designed for reading out the CMS silicon tracker signals transmitted by the APV25 analogue pipeline ASICs. The signals are transmitted to each FED via 96 optical fibres at a total input rate corresponding to 3 GBytes/sec. The FED digitizes the signals and processes the data digitally by applying algorithms for pedestal and common mode noise subtraction. At high luminosity the input data rate is reduced using algorithms that search for clusters of hits. Only the cluster data along with trigger information of the event are transmitted to the CMS DAQ system using the SLINK-64 protocol. All data processing algorithms on the FED are executed in large on-board FPGAs.



Primary side of FEDv1 (before OptoRx modules were assembled)

Architecture

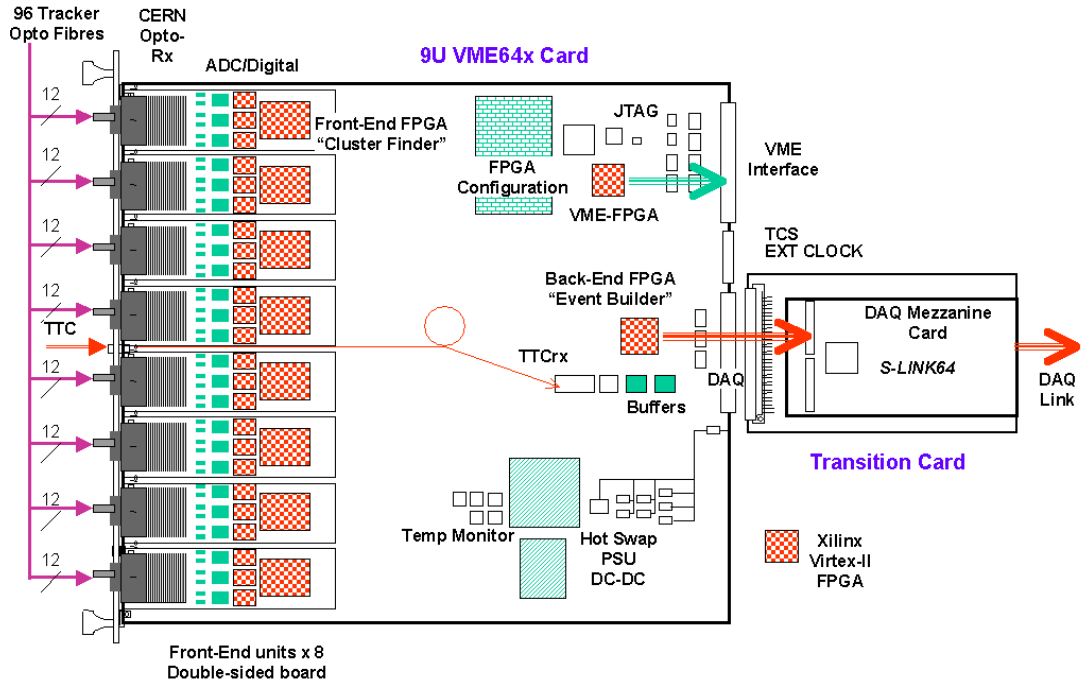
Each FED receives analogue data from eight 12-fibre bundles corresponding to 192 APV25s. The FED front end comprises of 8 identical units each receiving and processing the data from 12 fibres. One front end unit consists of:

- One Optical Receiver module [N] which receives the optical signals and converts them to electrical;
- 6 dual 10 bit ADCs;
- 3 x VIRTEX II XC2V40 (40K equiv gates) FPGAs, called delay FPGA, for clock distribution and clock phase adjustment;
- 1 x VIRTEX II XC2V 2000 (2M equiv gates) FPGA, called Front-End FPGA, which performs the pedestal subtraction and cluster finding.

The variable length clustered data fragments from all 8 Front-End modules are collected on point to point links (4 bits @ 160 MHz) by a single "Back-End" FPGA (XC2V2000). This builds a FED event for each trigger from the data fragments and formats and stores them in an external memory buffer (2 MBytes deep) to cope with fluctuations in the data rate. The event buffer is implemented with a pair of Quad Data Rate SRAMs.

Finally the FED data are transmitted to CMS DAQ via 400 MByte/sec copper links

using the S-LINK64 protocol implemented on standard DAQ mezzanine cards carried on VME transition boards. The same FED data buffer can alternatively be read via VME64x for test and monitoring purposes.



Block Diagram of FED

Hardware

Front Panel

Refer to Mechanical Drawing.

See also the LED description table.

PCB Form Factor

VME 64x 9U x 400 mm (ANSI VITA 1.3-1997)

14 Layers
(Signal/Gnd/Signal/Signal/Power/Signal/Power/Ground/Signal/Power/Signal/Ground/Signal)

Refer to Layers Drawings for details.

VME Connectors

Standard VME64x : P1, P0 & P2 (ANSI VITA 1.1-1997)

For detailed Pin Descriptions refer to Schematics Sheet 11

VME Interface

FEDv1 is currently implemented as a simple D32 VME Slave. The FEDv1 board layout has all the necessary signal lines needed for full VME64x master and interrupt functionality if a future

firmware upgrade is required.

Address Space : A32 Extended.

Size : 64 Kbytes.

Data Transfers : D32 ONLY (N.b. responses to D16/D8 accesses are undefined).

DMA : D32 transfers.

i.e. Following AM codes are permitted: 0F, 0E, 0D, 0B, 0A, 09

*FEDv1 does not provide arbiter functions and therefore each crate requires an arbiter card in Slot 1.

VME Base Address

FEDv1 uses the Geographical Slot Address pins to fix its base address. It does not implement VME64x CSR dynamic addressing functionality.

A31 - A22 mapped to 0

A21 - A16 mapped to slot address

A15 - A1 mapped to FEDv1 space

Examples:

FEDv1 in slot 2 address range : `$ 0002'0000 - $ 0002'ffff`

FEDv1 in slot 21 address range : `$ 0015'0000 - $ 0015'ffff`

Analogue Circuit

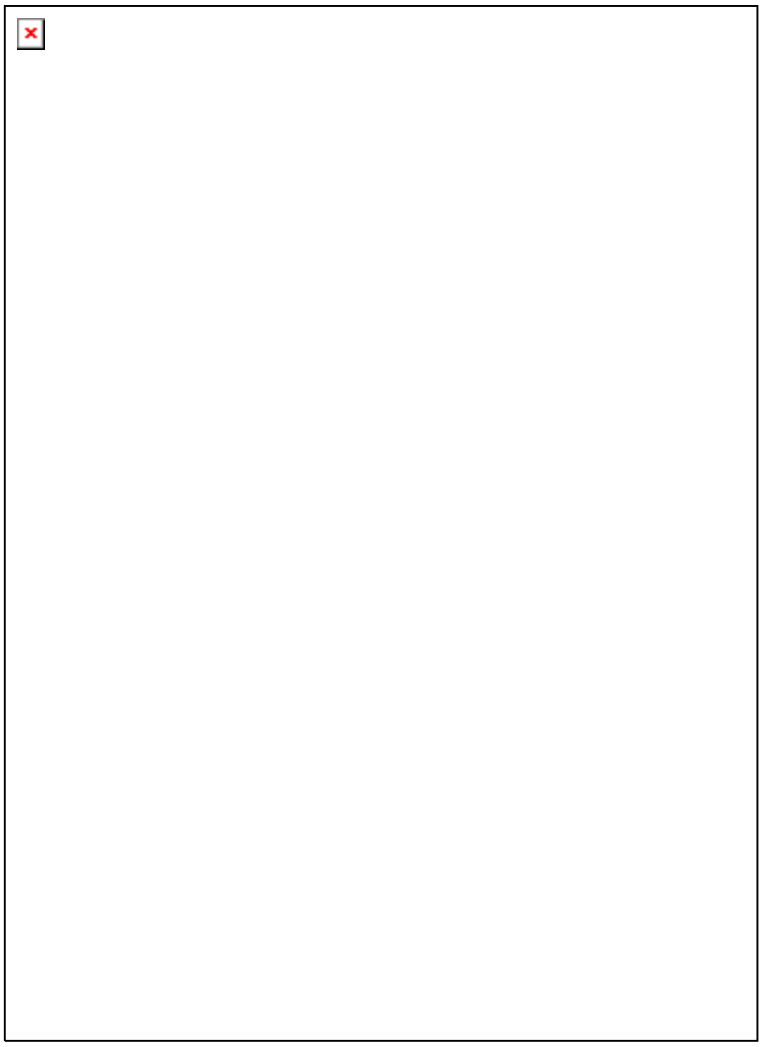
Jumpers

Refer to Assembly Drawings for details.

Clock Sources

FEDv1 can operate on 3 independent, exclusive clock sources selectable by software (see Figure 4) :

1. On board 40MHz Oscillator
2. TTC clock DeSkew 1. Firmware could in principle be reprogrammed to use TTC Clock40 or DeSkew2 if required.
3. Backplane LVDS input (**J0 9A+** & **9B-**)



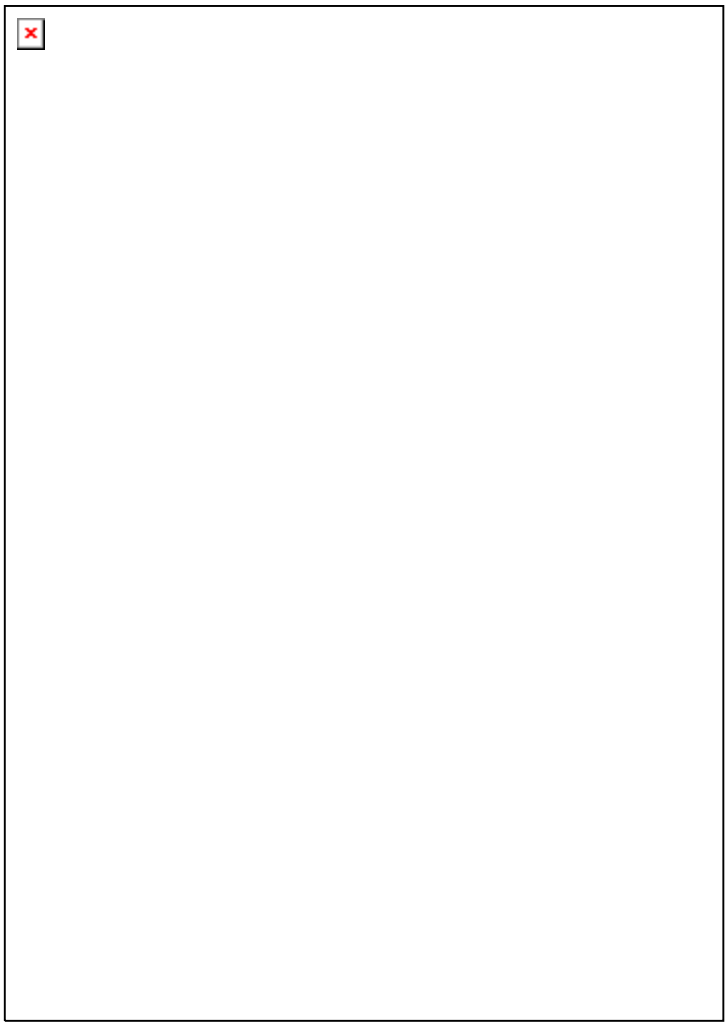
Clock Sources (click on image for full size picture)

Notes on clock changing:

1. If a clock change is successful a full reset is generated. After a full reset it is recommended to wait about 3 seconds before attempting to program registers to allow all the DCMs to relock.
2. If a clock change is unsuccessful no reset is generated and the board stays on the existing clock.
3. If the clock in use is lost the board reverts to Oscillator and a full reset is generated

Resets

There are several sources of resets on the FED.



Clock Reset scheme (click on image for full size picture)

Trigger Sources

FEDv1 logics can operate on 3 independent, exclusive trigger sources selectable by software :

1. Software generated.
2. TTC L1A
3. Backplane LVDS input (**J0 7A+** & **7B-**)

A filter is applied which will only accept legal CMS trigger patterns i.e. single trigger pulse of width 25 nsec with no immediate neighbouring pulses.

Examples:

‘0000100000’	counts as 1 trigger
‘0010010010’	counts as 3 triggers
‘0011000000’	counts 0 triggers (calibration request to APV ignored by FED)
‘0010100000’	counts 0 triggers (reset to APV) Resets FED BX counter.

Software

Refer to Software Pages.

Firmware

Refer to Firmware Pages.

Event Readout

Event Formats

JTAG and Boundary Scan

Frame Finding

Temperature Monitoring

Power Block

For detailed Pin Descriptions refer to Schematics Sheets 12,13 & 14.

References