CMS Tracker Electronics - TTC Interface

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This document details the CMS tracker electronics TTC interface. The TTC-B channel commands required for CMS running are defined for the FED and FEC boards. The commands will be sent from the TTCci (via the TTCex) as broadcast commands. After the broadcast command is decoded by the TTCrx the command is output on the Brcst<7:2> pins. The pins stay high until the next broadcast command is decoded. However, the bunch and event counter reset signals have their own dedicated pins, which only stay high for one clock cycle.

The broadcast commands, as well as the L1 accept signal on TTC channel A, can be delayed by coarse and fine steps. However, the commands cannot be delayed independently from the L1 accept signal.

The document is sectioned into 6 parts:
Section 1: TTC-B commands that the FED should decode and respond to.
Section 2: TTC-B commands that the FEC should decode and respond to.
Section 3: command format and command specific bit patterns.
Section 4: timing issues.
Section 5: additional notes.
Section 6: references.

1. TTC Channel B Commands Required for FED Operation

The commands the FED will decode are:

- **BCR** – Bunch counter reset. Note: This is a dedicated pin on the TTCrx chip. Note: currently a 101 on TTC-A will reset BCR (see note below).

- **ECR** – Event counter reset. This will reset both the event counter and the APV frame counter. This is a dedicated pin on the TTCrx chip.

- **RESYNC** – This is a *soft* reset. The RESYNC procedure is:
    1. When the FED receives a TTC-B resync command it will assert BUSY on TTS. It should then wait about 21μs to receive any more data from the APVs.
    2. The FED will then clear its buffers, error flags and counters (except bunch counter, event counter and APV frame counter).
    3. De-assert BUSY.

A RESYNC can be sent at any time by the run control system. However, it was decided that a RESYNC *should* be sent to the FED whenever the TTS OUT_OF_SYNC is set. This can be set, for example, when the FED buffers are close to overflow.

- **RESET** – This is a different TTC-B command from RESYNC, but will only cause the FED to perform a RESYNC. If more operations are required, they can be added at a later date.

- **TEST_ENABLE** – This command will indicate that the next event, corresponding to the next L1A signal, is a calibration event. The FED will set a flag in the event header to indicate calibration. There will be a trigger following the TEST_ENABLE after some pre-defined delay. The L1A event counter should be incremented when receiving this trigger. If TEST_ENABLE is issued during a physics run, normal physics triggers are inhibited during the above procedure.
  Note: Laser alignment calibration could take place during a physics run.

- **APV_CALIBRATE** – This command will indicate that the next event, corresponding to the next L1A signal, is a calibration event. The FED will set a flag in the event header to indicate calibration. There will be a trigger following the APV_CALIBRATE after some pre-defined delay.
  Note: APV_CALIBRATE will not be issued during a physics run.

- **APVE Address** – The APVE pipeline address is sent to the FED via a long format TTC-B channel broadcast command (low priority). The FED will set a register if this pipeline address disagrees with the observed one. An error flag will also be set in the event header.

Note: At present the FED decodes a 101 signal on TTC-A. This is a temporary measure, which was requested for the test beam. It will not be used in the final CMS system. The only signal decoded by the FED on TTC-A will be the L1A signal (a 00100).

2. TTC Channel B Commands Required for FEC Operation

The commands the FEC will decode are:

- **RESYNC** – This is a *soft* reset. When the FEC receives this command it will send a **101** signal to the tracker CCUs. This does not reset anything on the FEC itself.

- **APV_CALIBRATE** – When the FEC receives this it will send a **110** to the tracker CCUs.

3. Command Formats

The TTC channel B broadcast commands will be sent to the TTCrx chips in the following format:

0	0	8 bits (data)	4 bits (error checking)	1

The 8 bit data byte is in the following format:

Bit	**Name**	**Internal TTCrx action when high**	**Output pin name**
0	Bunch counter reset	Resets bunch counter	BcntRes
1	Event counter reset	Resets event counter	EvCntRes
<5:2>	Data	-	Brcst<5:2>
<7:6>	User message	-	Brcst<7:6>

There are 6 available bits for the user to define the TTC-B command. These bits are output on the Brcst<7:2> pins of the TTCrx chip. However, only the 4 data bits, Brcst<5:2>, are used to define which TTC-B command to send. The bit patterns that will define each command are listed below:

Command	**Bit Pattern Brcst<5:2>**
RESYNC	0101
RESET	0110
TEST_ENABLE	0010
APV_CALIBRATE	1011

4. Timing and post TTC-B command issues

For the FED board only: The TTCrx broadcast command will be sent at least a few clock cycles before any L1A is sent. When the FED receives a L1A it will check the status of the TTCrx Brcst pins, and then perform the appropriate action.

For both the FED and FEC: After a TTC-B command is sent, possibly followed by a L1A, a 0000 broadcast command is sent a few clock cycles later from the TTCci (before the next L1A). This will clear the TTCrx Brcst pins so that they do not retain the state in which they were placed by the previous TTC-B command.

5. Additional notes

Only FED version 2 boards are able to decode the signals on the TTCrx Brcst pins. The FED version 1 boards (which will not be used in CMS) only have a fraction of the TTCrx pins connected.

6. References

1. *TTCrx Reference Manual - A Timing, Trigger and Control Receiver ASIC for LHC Detectors,* J. Christiansen, A. Marchioro, P. Moreira and T. Toifi. See http://ttc.web.cern.ch/ttc/

2. *CMS L1 Trigger Control System,* Editor: J. Varela. CMS NOTE 2002/033.