



# FRL SERIES: test bench 1

Operator name  
Bel Nicolas

Serial Number  
3DA0010020010000001 + - DB Refresh

Program  
OK

Board used  
FRL card (CPCI) ver1.0

Working directory  
C:\ Program FPGA

Standard input  
dir\n OK

Standard output

DB Comments  
test passed - 5/4/2004 3:12:15 PM - Bel Nicolas

STOP

ADD to DATABASE

Database parameters file (\*.udf)  
D:\development\LW\_DB\_connect\

**Manual Measurements**

Visual test DB

Switch/Strap

5 Volts

3,3 Volts

2,5 Volts

1,8 Volts

5 V current mA

3,3 V current mA

2,5 Volts

1,8 Volts

DB

2

3

2.5

1.5

**this bench will be used for Slink64, FRL, FMM and trigger distributor boards**

- manual measurements of electric integrity
- serial number programming
- FPGA programming
- all results inserted in database



## FRL SERIES: test bench 2

### Automatic test system

- JTAG chain test for PCI programming
- integrity check: read-write test, memory test
- verify Slink autotest
- verify all connections (input, output, internal PCI bus, zbt memory ...) through a quick dataloop run
- all results inserted in database

