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Performance Verification of the CMS Tracker FED Analog Front-End Electronics

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Abstract

Preliminary version

1 Introduction

Testing of the FED has been carried out at CERN in order to assess the dynamic performance of the CMS Tracker FED's [1] analog front end electronics. A pulse generator is used to provide a well-controlled input. This allows for accurate measurement of rise and settling times to be made, which is otherwise impossible using pulses (ticks) produced by the APV25 chip [2] in the final readout system configuration.

A schematic representation of the CMS Tracker FEDv1 front end analog electronics is shown in Figure 1. Only one signal path (i.e. one channel) is shown for illustrative purposes. The analog optoelectronic receiver (ARx12) converts the incoming light into a current that flows through a load resistor, hence producing a single-ended voltage signal. This is then converted to a differential signal by the EL2140C differential driver IC. A voltage divider stage halves the signal levels to match the input range of the ADC (AD9218).

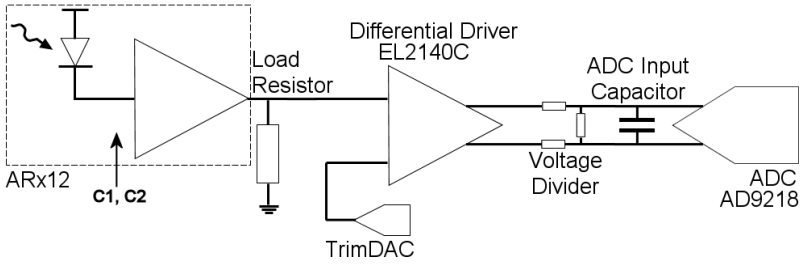

Figure 1: The CMS Tracker front end analog electronics

The ARx12 was designed with a user-selectable capacitance between the pin diodes and the input of the current-mode amplifier. Hence, two switches (C1 and C2) allow tuning of the pulse response to achieve the best dynamic performance in terms of rise and settling time. There are four available settings (800, 1000, 1200 and 1400fF). The dynamic behavior of the ARx12 has been tested rigorously at CERN, both during the qualification and production phases of the device. The vast majority of receiver modules achieve optimum dynamic performance at the 1000fF setting in the production test fixture. A correlation between optimum capacitance setting (C_{ARx}) and bandwidth measured by the production has been found [3]. It was hoped that this would allow the appropriate C_{ARx} setting to be known a priori when commissioning the final Tracker readout system. This is an important conclusion, since there is currently no way of performing precise dynamic tests when the final system is in place. Hence, the bandwidth-C_{ARx} correlation provided the first incentive for the tests described in this document. Before recommending nominal C_{ARx} settings for the final system, it is necessary to verify that receivers mounted on FEDs behave in the same way as in the production test fixture at CERN.

The first set of results revealed that the differential driver introduces some overshoot to the incoming pulses (§2.2) Therefore, modules that perform best at 1000fF in the production tests should be set to 800fF when mounted on FEDs. Since this is the lowest C_{ARx} setting available, flexibility is compromised. This potentially means that the (few) modules that perform optimally at 800fF in production tests, may not meet the dynamic specifications when mounted on the FEDs (since is no lower C_{ARx} setting available to compensate for the extra peaking). In order to remedy this situation and achieve a typical setting of C_{ARx}=1000fF, it was suggested that a higher value capacitor at the input of the ADC (C_{ADC}) would slow down the pulse and therefore reduce the overshoot.

A Monte Carlo simulation of the gains of the optical links has shown that, at room temperature, the gain is higher than expected [4]. This means that nearly all the links would have to be operated at the lowest gain setting of the Analog OptoHybrid in order to achieve the specified gain and resolution for the system. This problem is further compounded by the fact that at the nominal Tracker temperature of -10˚C, the gains of electronic and optical components are expected to increase further. Simulations incorporating temperature effects were also carried out, and the results have shown that the specifications of dynamic range and resolution will not be met in the final system, due to an expected gain increase of approximately 30% [5]. One way of reducing the gain and recovering the lost dynamic range would be to change the FED's ARx12 load resistor (R_L), whose value is affects the gain of the complete readout link. It has been shown that lowering the value to 62Ω (from the nominal 100Ω) will achieve the required gain compensation. The simulation model was also used to show that, with this load resistor value, a large range of temperature-related gain increase can be tolerated as far as the readout system specifications are concerned.

Hence a second set of measurements was carried out on a FEDv1, 36 channels of which were modified with:

- Six different C_{ADC} values (4.7, 10, 22, 33, 47 and 68pF) in order to reduce the overshoot introduced by

the differential driver IC, hence making 1000fF the typical C_{ARx} setting.

- Three different R_L values (56, 75 and 100Ω) in order to assess the impact of gain compensation on the dynamic performance.

In all, 18 different combinations of load resistor and ADC input capacitor were mounted on 36 channels of the modified FED. The results are presented in §3.2.

2 FEDv1 Tests

2.1 Test Setup

Figure 2 shows the test setup used. It should be noted that only one FED channel can be tested at a time. A LeCroy 9210 pulse generator was used to provide a differential input to the AOH. As in the Tracker Lab reference link measurements, the period was set to 100ns, with 50% duty cycle. 800mV differential amplitude was used with a common mode of 1.25V. The pulse generator was controlled by a portable PC via a USB-GPIB interface. The PC was also equipped with a USB-I^2C for setting the AOH gain and laser bias. The laser was deliberately biased high, since it was impossible to run the usual automatic link tuning procedure. This limitation was due to the fact that, in this setup, it was not possible to interface the AOH to the FEC CCU that is normally used for control purposes with the conventional setup (i.e. when the APV is used to send data to the FED). To verify that the optical pulse out of the AOH was not being clipped, it was observed on an oscilloscope using an optical head, and the biasing performed 'by eye'. The AOH gain was set to 5.0mS, the lowest gain setting available. On the FED side, the ARx12's X0-X5 settings were set to the nominal value (switches X0, X2 on). For the electrical probing tests, the pulse generator was set to trigger itself automatically and continuously. Thus, a continuous pulse train was output to the AOH. Waveforms of the pulses at various test points were recorded on a LeCroy LT354 oscilloscope, using differential and single-ended probes.

For data captured by the FED, the Trigger Sequencer Card (TSC) was used to provide a synchronous trigger to both the FED and the pulse generator. On receipt of a trigger, the pulse generator was set to output a pulse after a delay of 2µs. The FED was in scope mode, capturing data points every 25ns for a time window of 7µs (280 points), thus ensuring that the incoming signal would be visible inside the time frame captured. The FED incorporates a 'fine delay skew', which skews the ADC sampling clock in 32 steps within a 25ns period[1]. The fine delay was used to obtain data points spaced apart by less than 1ns. The FED was programmed to capture 7µs of data (one 'event') for each of the fine delay skew settings. The pulse was then reconstructed by interleaving the data corresponding to the 32 skew settings. The TSC sent 100 triggers per skew setting, and hence 100 events were captured. Each data point was then determined by averaging over all the events.

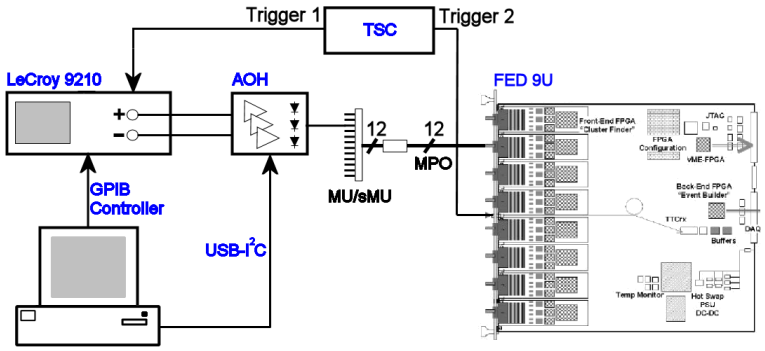

Figure 2: Test setup used for the dynamic characterization of the FED

The configuration used to set up the triggers is shown in Figure 3. The triggers arrive almost simultaneously to the FED and pulse generator (at ~1µs on the scope trace), while a pulse is output from the AOH 2µs later. This ensured that the pulse was near the middle of the FED's data capture window.

[1] This was the case at the time these tests were performed. The latest FED software maps the 32 fine skew delays to 25 settings, so that each skew setting corresponds to approximately 1ns steps.

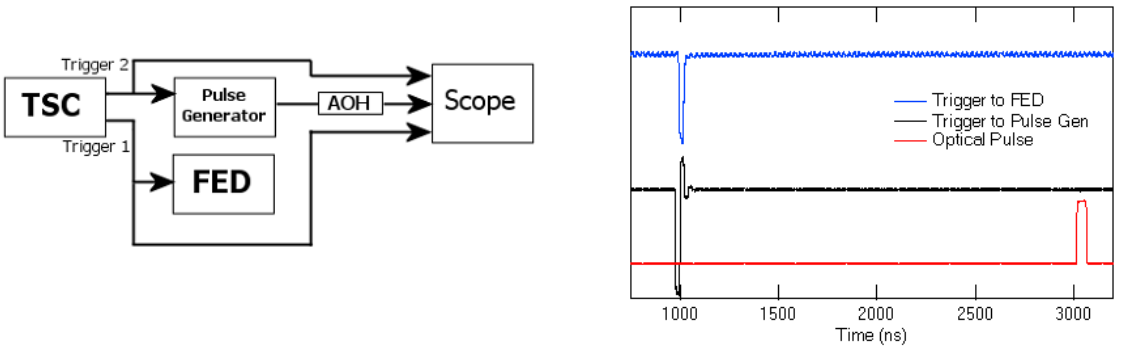

Figure 3: Setting up the triggers to the pulse generator and FED (left) and oscilloscope traces showing the relative timing of the triggers and of the AOH output pulse (right).

2.2 FEDv1 Test Results

Figure 3, left, shows the electrical input to the AOH, obtained using a differential probe. The resulting optical signal at the output of the AOH was viewed on the scope using an optical head (Figure 4, right).

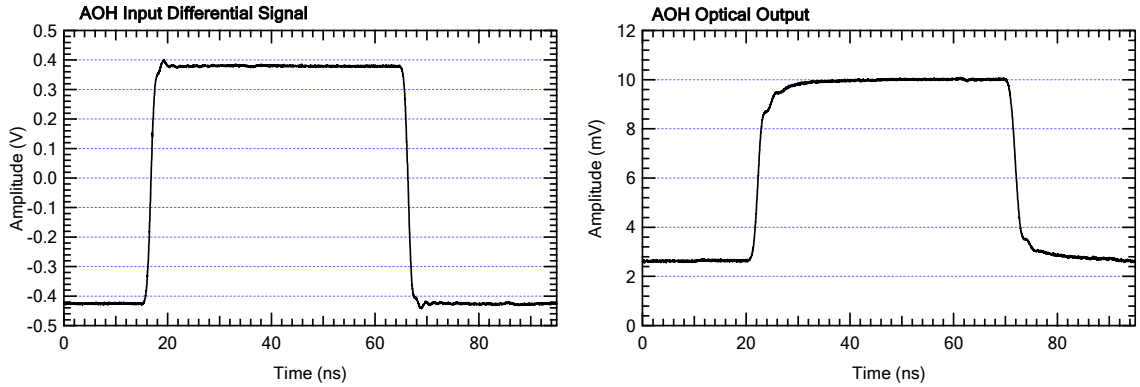

Figure 4: Differential Input to the AOH obtained using a differential probe (left), and corresponding pulse at the output of the AOH connected to an optical head.

The FED was probed electrically at the following points (Figure 5):

- ARx12 load resistor (single-ended)
- Output of the differential driver (differential)
- ADC input capacitor (differential)

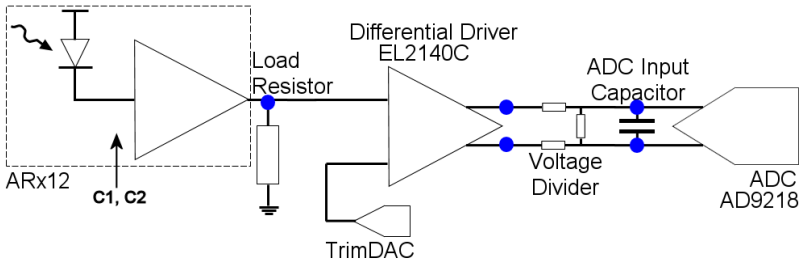

Figure 5: Showing the FED analog front end electronics. The blue circles indicate where the FED was probed.

Figure 6 shows the signals obtained for all four capacitance settings of the ARx12, probed at the load resistor (i.e. the optical receiver's output). The settling time specification of 15ns is illustrated by the dotted line. As expected, the result is very similar to what is seen in the ARx12 production tests performed in the lab at CERN. The effect of increasing the capacitance setting is to speed up the pulse, as is clear by the rise time decrease. The overshoot is also affected, which has a dominant influence on the settling time. Clearly, this particular channel performs best at a capacitance setting of 1000fF, where the settling time is at a minimum and well within the

15ns specification. The vast majority of optical receivers behave in the same way, giving confidence that the tested FED channel is a typical case of what can be expected in the final system. This is illustrated in Figure 7, which shows the settling time plots of all channels of all 10 modules of ARx12 production batch R4. The vast majority of channels perform best at 1000fF.

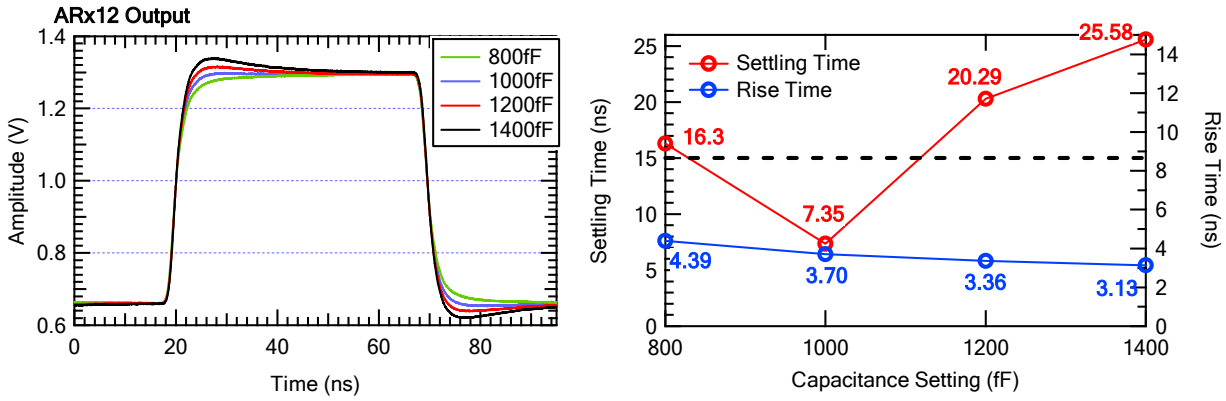

Figure 6: Single-ended signals at the load resistor of the ARx12 for all four ARx capacitance settings, with the corresponding settling and rise times shown on the right.

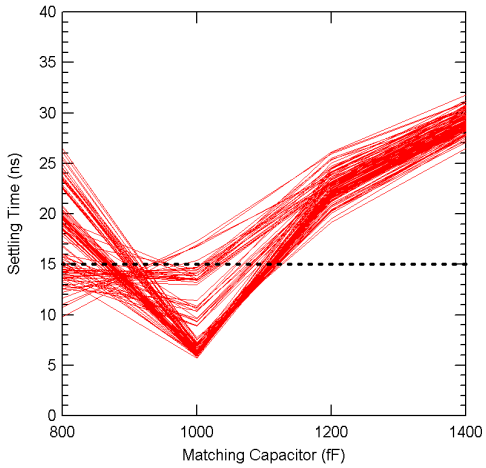

Figure 7: Settling time plots for all channels of the 10 production test modules belonging to batch R4.

Figure 8 shows the waveforms obtained when placing the differential probe on the output of the differential driver IC. The ringing observed after the rising edge of the pulse is probably due to the way the probe was attached to the IC's pins. Extra attached wires (2-3cm long) had to be connected to the probe's ends to enable probing between the tiny pins. An increase in the overshoot of the pulse is clearly visible. This is mirrored in the settling time plot, where the minimum settling time is now achieved at a capacitance setting of 800fF. Using a single-ended probe, the signal on each branch of the differential driver was looked at (Figure 9). The extra peaking on the differential signal appears to be due to the asymmetry of the individual branch signals.

Probing the input of the ADC proved very difficult, and it was impossible to maintain a consistent contact across the pins of the ADC input capacitor. The results are nevertheless included for completeness (Figure 10). Despite the uncertainty of the probing, they do seem to confirm the additional overshoot observed at the output of the differential driver.

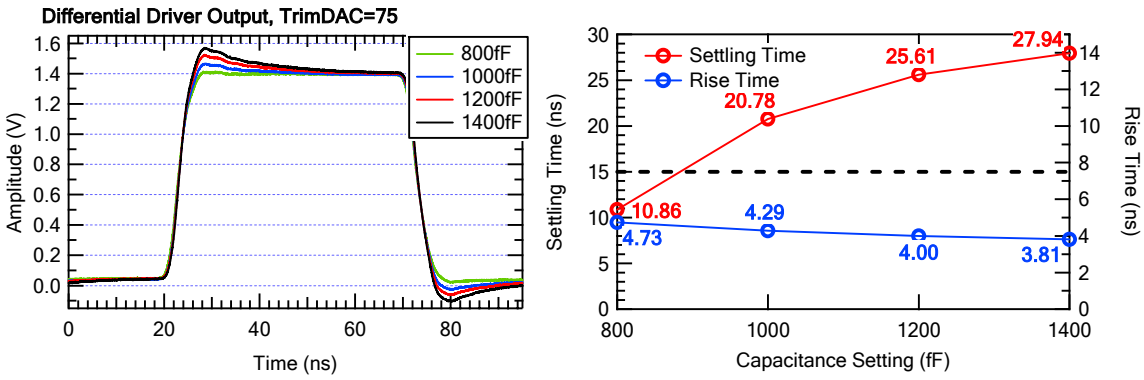

Figure 8: Signals at output of differential driver IC for all four ARx12 capacitance settings (left), with corresponding settling and rise times (right).

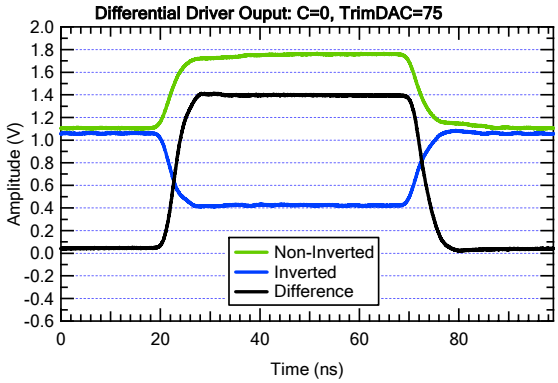

Figure 9: Signals obtained by probing each branch of the differential driver output using a single-ended probe. Only one ARx12 capacitance setting was used.

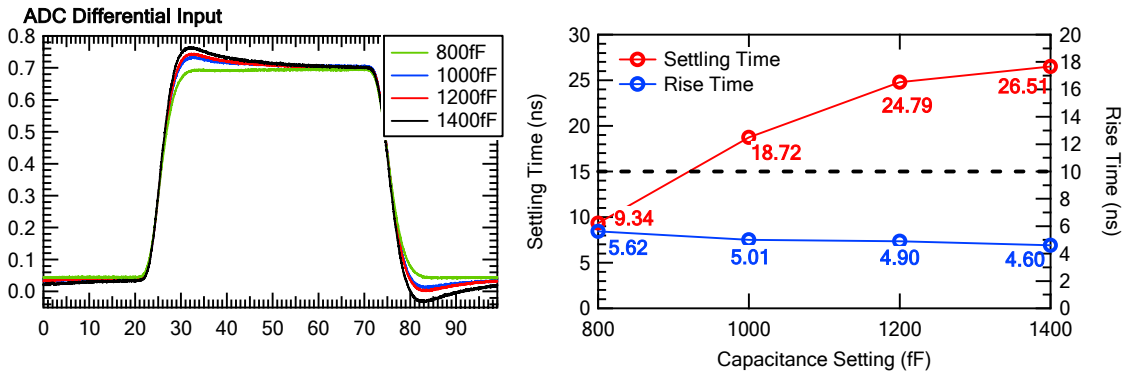

Figure 10: Signals at the input of the ADC for all four ARx12 capacitance settings (left), with corresponding settling and rise times (right).

After probing electrically, the FED was used to capture data and the incoming pulses were reconstructed as described section 2. The results are shown in Figure 11, which confirm that the best ARx12 capacitance setting for this channel is 800fF. It is also evident that there is a significant slowdown of the pulses at the ADC. The rise times are now as much as 1.5ns higher than in the preceding stage. This could be attributed to the capacitance seen by the signals due to the 4.7pF capacitor across the differential inputs, as well as the additional internal capacitance of the ADC (typically ~3pF). Moreover, while the analog bandwidth of the ADC is quoted at 300MHz, there is no specification for the slew rate, which could ultimately be a limiting factor for the rise time of the pulses.

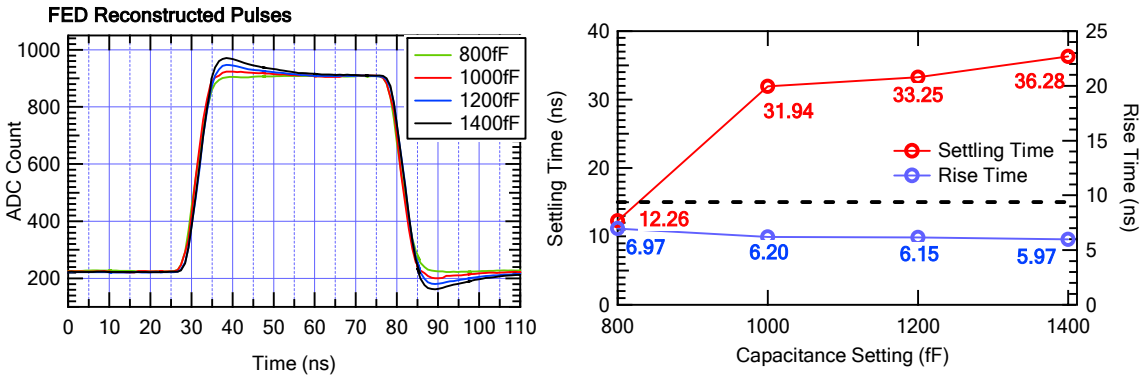

Figure 11: Pulses obtained by reconstructing captured FED data (left). Settling and rise times are shown on the right.

The results have shown that the overshoot of the input pulses is increased after the differential driver IC stage. Consequently, when selecting the best ARx12 capacitance setting for a given receiver module, the effect of the FED's front end analog electronics should also be taken into account in order to achieve the best possible dynamic performance. The results suggest that modules showing best capacitance settings of 1000fF in the production tests (i.e. when looking at the output of the optical receiver), should be set to 800fF to compensate for the extra peaking introduced by the FED. Clearly, this is not an ideal situation, since operating at the lowest capacitance setting means less flexibility in the final system. The proposed solution to this problem was to increase the value of C_{ADC}. It was hoped that this would slow down input signals, and hence reduce the overshoot.

2.3 Linearity

With the existing test setup, it is not possible to control the AOH with the software used the rest of the hardware. Hence, a fast, automated linearity measurement based on successively measuring the output from the FED as a function of laser bias setting was not possible. Another conventional method for measuring linearity involves using an arbitrary waveform generator to input a slow differential ramp to a properly biased AOH. It requires developing appropriate FED software and accurate synchronization with a trigger system to ensure data is acquired at the right intervals. Due to time limitations, this was not realized.

Nevertheless, a basic attempt at measuring the full readout link linearity was made. The pulse generator was used to input DC values to the AOH. Two non-inverting channels on the pulse generator were used for this purpose. Channel A was connected to the non-inverting input to the AOH, and channel B to the inverting input.

Both outputs were set to output the smallest pulse allowed (50mV), with the shortest possible duration (1% duty cycle, maximum rise and fall times, with a period of 500ns). The resulting output from each channel is, essentially, a DC level with a short duration 50mV 'kink' appearing every 500ns. In fact, since the two pulse generator channels are subtracted by the differential amplifier in the AOH, the 'kinks' disappear, producing an almost flat resultant DC level (Figure 12).

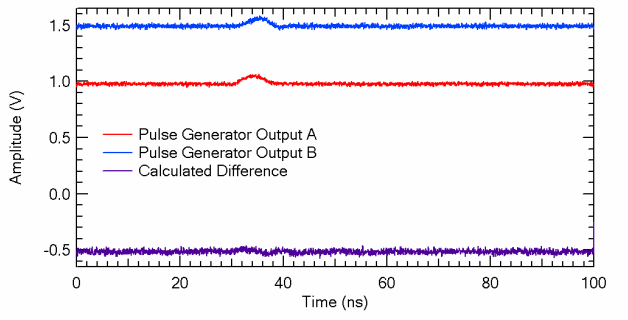

Figure 12: Pulse generator outputs as seen on an oscilloscope. The purple trace is produced by subtracting one channel from the other, thus emulating what happens at the input to the AOH.

Figure 12 shows the first DC level that was input to the AOH (-0.5V). In order to measure linearity, the DC input to the AOH was swept from -0.5V to +0.7V, in steps of 40mV. This was done by adjusting the individual outputs of each pulse generator channel, controlled by the PC. For example, to obtain the next DC input of -0.46V, one sets pulse generator channel A to 1.02V and pulse generator channel B to 1.48V. Hence at the differential amplifier of the AOH, the result is 1.02 -1.48 = -0.46V. This was repeated up to a 0.7V input. For each DC input point, the FED acquired and averaged 280 points of the output every 25ns. A total of 31 measurements were this way.

It should be noted that this measurement was made manually with no automated trigger system to synchronize the FED with the pulse generator. A LabView program was written to allow the user to successively increment the pulse generator outputs, while the FED was ordered to take data separately. Hence, the time between measurement points was not constant, and, more importantly, the total time taken for this test was of the order of a minute. Fluctuations in ambient temperature, or errors due to self heating of the laser at higher DC inputs therefore could not be avoided.

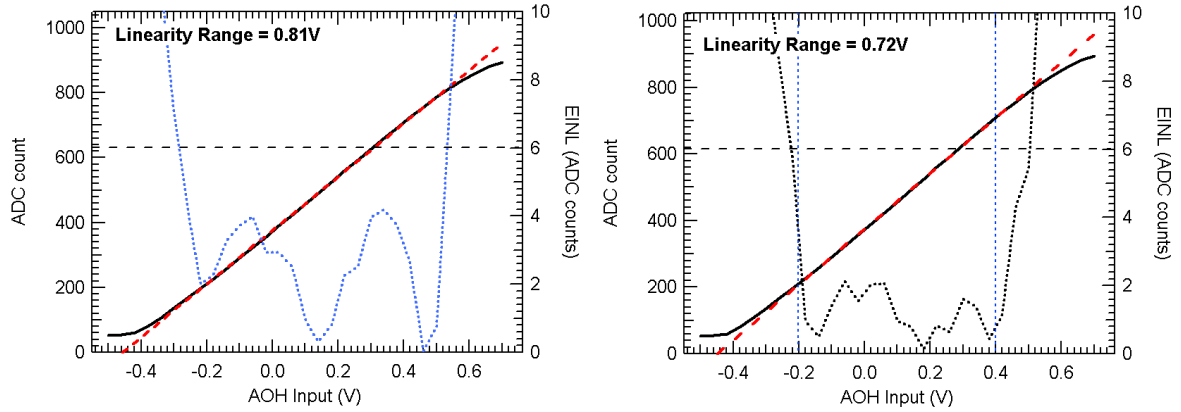

Figure 13: Linearity computed from the deviation of the straight line fit over the range -0.2V to 0.4V (left) and -0.3V to 0.3V (right). The horizontal dotted line indicates the point at which the EINL (Equivalent Input Non-Linearity) is 1%.

The Equivalent Input Non-Linearity (EINL) is normally computed by fitting a straight line to the data over the range of the specified input to the readout link (i.e. -0.3V to 0.3V), as seen in Figure 13, left. The deviation from this line as a percentage of the input range (0.6V) gives the EINL. However, for this measurement, the AOH was deliberately biased low (I^2C setting 20) so that the laser threshold is clearly visible at the output. This can be seen at approximately -0.4V input. Consequently, the linear range (i.e. the range for which EINL < 1%) begins slightly after -0.3V input. For this reason, a second calculation was performed, this time by fitting a line from -0.2V to 0.4V, to compensate for under-biasing the laser (Figure 13, right). To enable a fairer comparison, the optical link should be properly tuned using the usual automated method before measuring linearity.

Despite the uncertainty of the method, the results look very promising. Equivalent Input Non-Linearity is better than the specification of 1% for an input range greater than 600mV for both calculations. Ambient temperature effects, as well as laser self-heating most likely degrade the results.

3 Modified FEDv1 Tests

A FEDv1 was modified for testing purposes. Eighteen combinations of ADC input capacitors and ARx12 load resistors were mounted on 36 channels, replacing the current values (C_{ADC}=4.7pF and R_L=100Ω). The aim of this exercise was to determine whether changing C_{ADC} would reduce the overshoot in the pulse response resulting in a typical optimum ARx12 capacitance setting of 1000fF. The values mounted on the modified FED were: 4.7 (current value), 10, 22, 33, 47 and 68pF. The channels with the 47pF capacitor did not function correctly (perhaps due to the wrong component used); therefore these are omitted from the results. It will become clear, from the results, that this had no impact on the conclusions reached.

A simulation of the optical readout links has shown that the gain in the final system at operating temperature will be higher than expected. In order to recover the lost dynamic range, it will be necessary to lower the value of R_L by ~40%. A lower load resistor will speed up the pulse response, and it was therefore necessary to check if the overshoot would be worsened as a result. Hence, three different resistors were used on the modified FED: 56, 75 and 100Ω (current value).

Table 1 shows the values of the components used per FED channel. An RC parameter has been specified, which is simply the product of the R_L and C_{ADC}. While this is clearly not a real physical quantity, it provides a useful way of visualizing the results, since the effect of increasing either of the two values is to slow down the response of the system.

Table 1: R_L and C_{ADC} values on the modified FEDv1

FED Channel	R_L (Ω)	C_{ADC} (pF)	RC	FED Channel	R_L (Ω)	C_{ADC} (pF)	RC	FED Channel	R_L (Ω)	C_{ADC} (pF)	RC
0	100	4.7	470	**12**	75	4.7	352.5	**24**	56	4.7	263.2
1	100	4.7	470	**13**	75	4.7	352.5	**25**	56	4.7	263.2
2	100	10	1000	**14**	75	10	750	**26**	56	10	560
3	100	10	1000	**15**	75	10	750	**27**	56	10	560
4	100	22	2200	**16**	75	22	1650	**28**	56	22	1232
5	100	22	2200	**17**	75	22	1650	**29**	56	22	1232
6	100	33	3300	**18**	75	33	2475	**30**	56	33	1848
7	100	33	3300	**19**	75	33	2475	**31**	56	33	1848
8	100	47	4700	**20**	75	47	3525	**32**	56	47	2632
9	100	47	4700	**21**	75	47	3525	**33**	56	47	2632
10	100	68	6800	**22**	75	68	5100	**34**	56	68	3808
11	100	68	6800	**23**	75	68	5100	**35**	56	68	3808

3.1 Test Setup

There were various differences in the testing procedure of the modified FED that should be noted. Firstly, the input pulses were set to 300mV differential, which is equivalent to the height of a 3MIP signal in a thin (320μm) silicon detector. This ensured that the entire signal being studied was within the linear range of the readout link (~600-800mV). The pulse length was set to 200ns, to gain more confidence in determining the final value of the signal (for the settling time calculation). When capturing data with the FED, 10 ‘events’ per skew setting were used, compared to 100 previously. This was due to a compromise between confidence in the error on the data and time constraints, since the setup can only test one channel (out of 36) at a time. Finally, only FED reconstructed data was used, since electrical probing on all 36 channels was not practically feasible, and unnecessary.

3.2 Modified FEDv1 Test Results

Figure 14 (left) is an example of the data captured by the FED. All pulses were normalized for analysis purposes. The corresponding settling and rise times are shown in the same figure (right). Clearly, the pulse settles fastest at 800fF. The results are similar to what was observed in the previous tests on the non-modified FEDv1, which had the same R_L and C_{ADC} values.

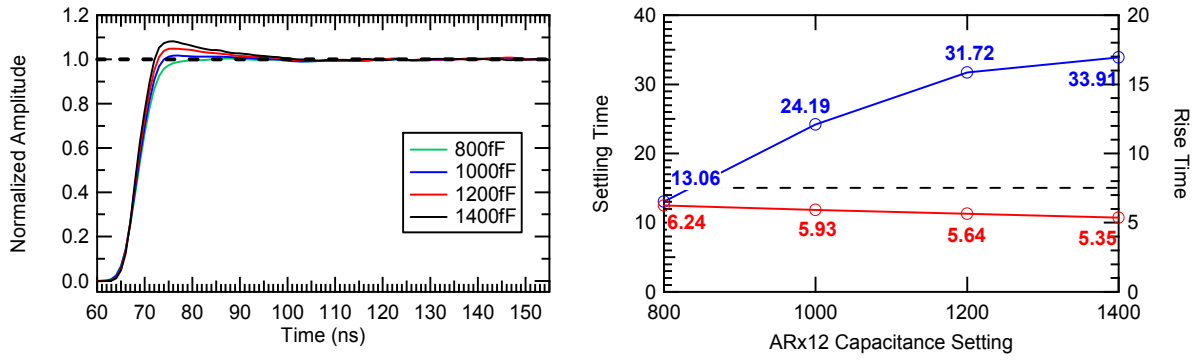

Figure 14: FED channel 0 reconstructed pulse and extracted rise and settling times as a function of ARx12 capacitance setting. Component values on this channel: R_L=100Ω, C_{ADC}=4.7pF

In order to better understand the detailed results that follow, the effect of increasing the ADC input capacitance will be first illustrated. To this end, channels with load resistors of 75Ω and the five different working ADC capacitors were picked. The pulses are plotted only for one ARx12 capacitance setting (1000fF), but the same conclusions can be reached with any of the four settings (Figure 15).

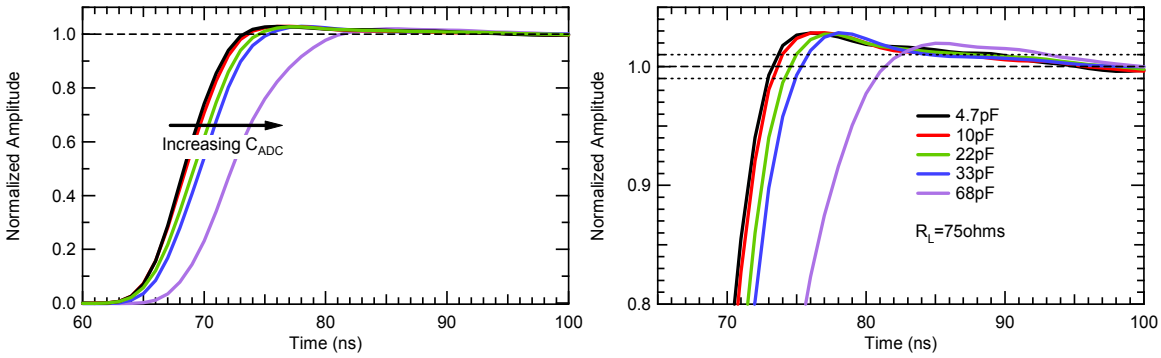

Figure 15: Effect of increasing ADC capacitor value with a constant load resistor value (75Ω). Only pulses obtained with an ARx12 capacitance setting of 1000fF are shown.

It is clearly evident that increasing the ADC capacitor severely affects the rise time. The overshoot is reduced somewhat, but this is only obvious for the 68pF capacitor. The effect is negligible compared to the large increase in rise time, and hence the settling time is made worse.

Figure 16 shows the settling times of every tested channel as a function of RC product. Results are plotted separately for each ARx12 capacitance setting. The different marker types correspond to each of the three load resistor values; the effect of increasing the ADC capacitor for a given load resistor value can therefore be seen by following the points with the same marker type along the positive direction of the x-axis. There are two points per RC value, since the modified FED has 2 channels per combination of load resistor and ADC capacitor (see Table 1). Figure 17 shows the rise times as a function of RC value. Here the effect of increasing either of the two component values is obvious, with the rise time increasing proportionally.

From the settling time plots it is immediately clear that increasing the value of C_{ADC} will not succeed in changing the best ARx capacitance setting to 1000fF. The pulses settle best at 800fF, regardless of the component values used. Moreover, the rise time is significantly increased with higher C_{ADC} values, masking any improvement in the overshoot of the pulse. Hence, in general, the settling time remains the same or gets worse.

As expected, decreasing the value of R_L speeds up the pulse. This is readily seen in the rise times of Figure 17. Though it is difficult to identify a clear trend from the settling time results, there is no evidence that performance is compromised when using lower resistor values. If anything, there seems to be a general improvement in the settling time.

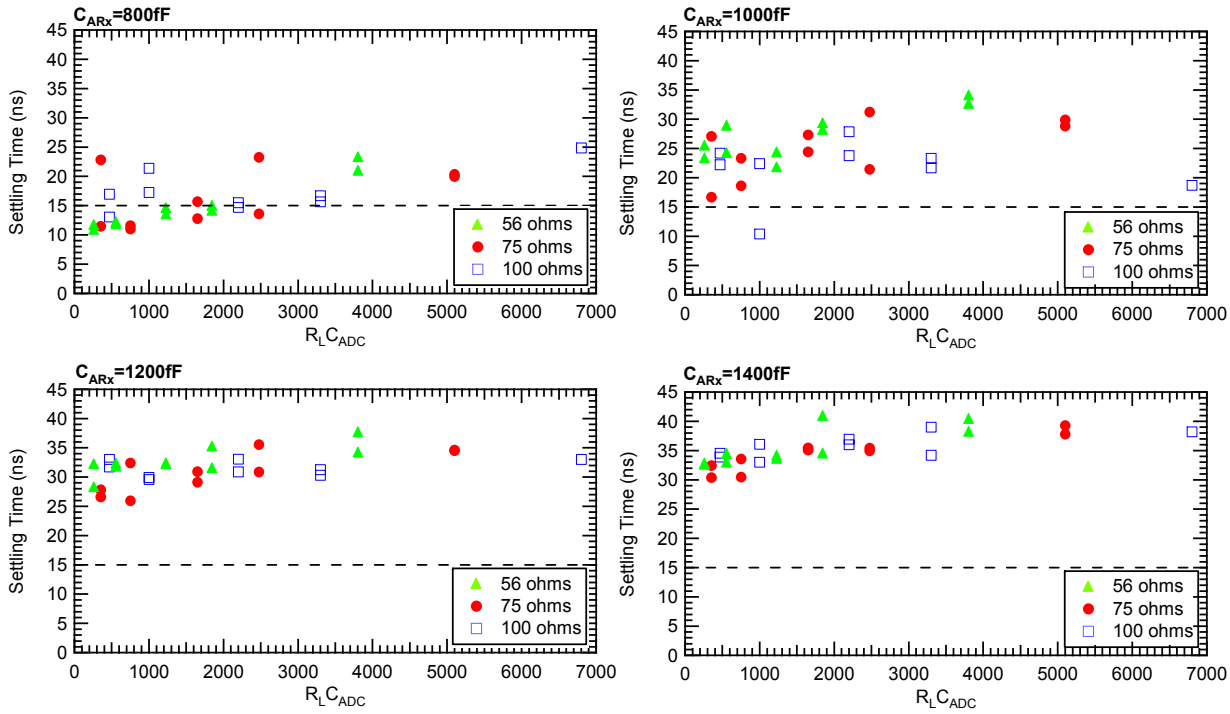

Figure 16: Settling time as a function of RC value for all four ARx12 capacitance values.

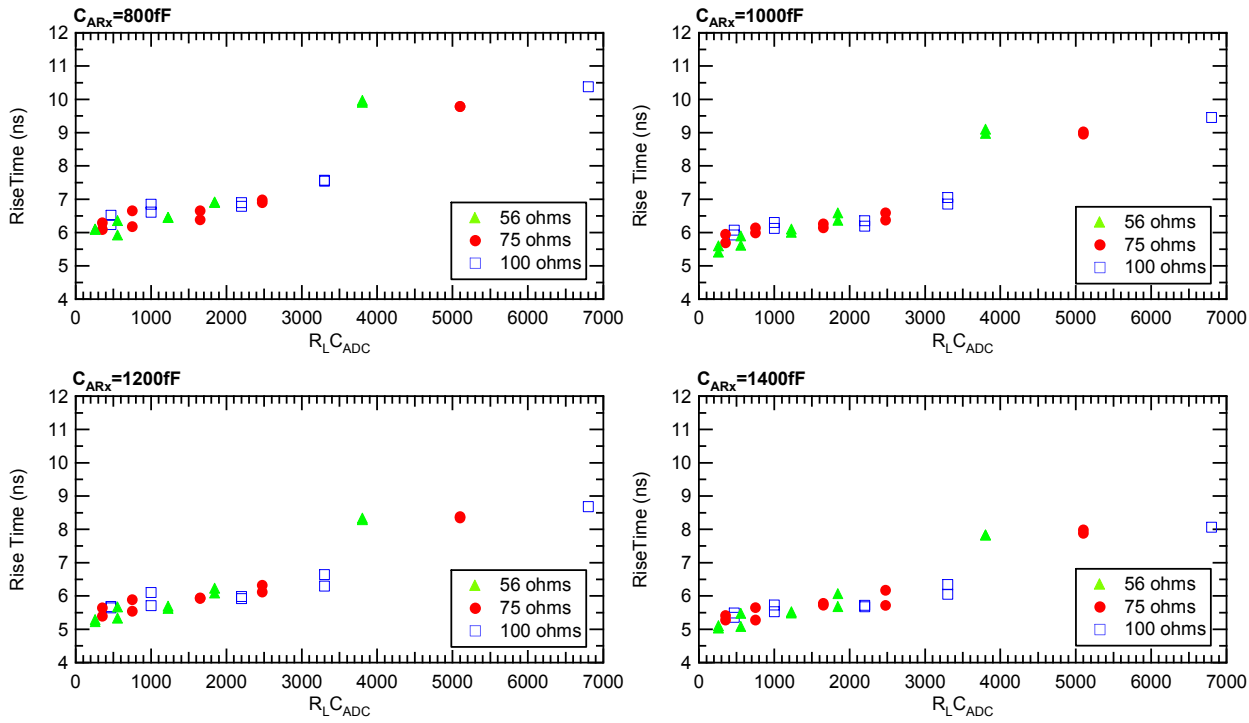

Figure 17: Rise time as a function of RC value for all four ARx12 capacitance values.

4 Conclusions

The results show that there is no reason to change the ADC input capacitor from the current value of 4.7pF. The overshoot on the pulses is not reduced and no improvement in settling time is observed with higher C_{ADC}. On the other hand, lowering the load resistor will not pose any problems for the dynamic performance of the system. Therefore a 62Ω resistor can be used, as suggested by the link gain study. A new FEDv2, which will include the recommended values, will be shipped to CERN for validation testing in January 2005.

5 References

[1] J.A. Coughlan *et al.*, "The CMS Tracker Front-End Driver." *9th Workshop on Electronics for LHC Experiments*, CERN/LHCC/2003-006, pp.255-259. (2004).

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