

## Project Monitor Form

**Project:** CMS FED

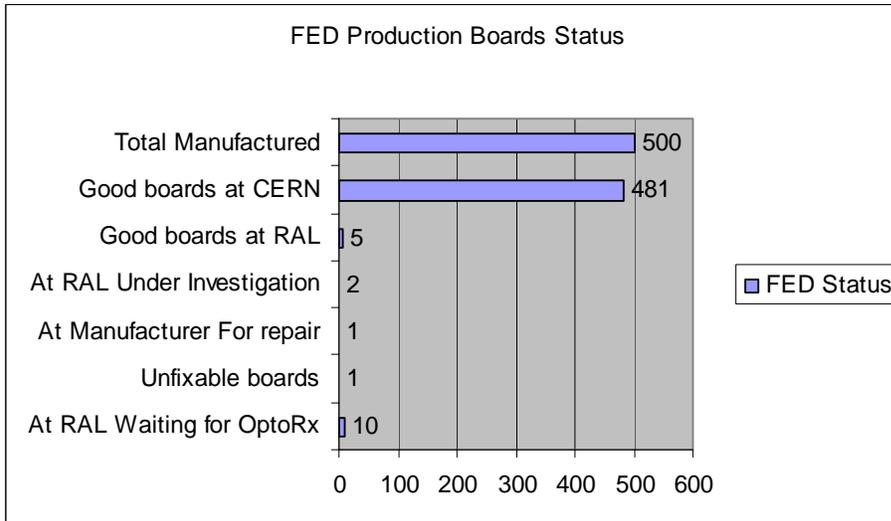
**Date:** Friday 31 August-2007

**PMF number:** 68

**Sheet:** 1 of 2

Project Implementation phase.

### FED Production



Full details in Production [spreadsheet](#).

### FEDs

Ivan has successfully recovered ORx from the unfixable board and placed on an unpopulated production board. Latter board then passed all tests.

No further boards have been returned to RAL.

FPGA loading problems (on preproduction board) in Finland may have been due to 5V Osc. Osc now replaced with correct 3V device.

Several of the old prototype FEDv1s have been tracked down and returned from Exception (the ORx were already removed)

Following the move of the RAL Test rig Ivan found 2 more trays of ORx. These have been fitted on unpopulated boards.

Recovery of the Test Rig at Exception is put back a few weeks owing to pressure of work at RAL. This is not urgent.

### CERN Installation and Commissioning :

Operation at the Tracker Integration Facility TIF was stopped in July. All but a couple of the FEDs have now been removed from TIF racks and sent to USC.

The TIF run is considered a great success with several million cosmic events recorded (by the FEDs) at various tracker temperatures.

Ivan and Oz have completed the installation of the last 3 rack of FEDs. We have all the 440 FEDs and the Transition Cards in 31 crates. All the PC's for these FED crates are in the PC rack S2B17-18. We have to wait for the pc experts to install the necessary network connections and the OS to these PC's before we can use them.

This means that since August 3rd:

### **All 446 FEDs are now installed at USC with SLINK connections!**

The DAQ is in good shape (see communication below). Further Global DAQ tests are scheduled for next week. Note these tests are with Simulated FED FAKE Data.

#### DAQ Commissioning Tests Jon Fulcher 8<sup>th</sup> August

Today with the help of Christoph Schwick and the DAQ guys we successfully tested 5 whole crates of FEDS in a single configuration using the final DAQ cluster. We succeeded to write to disk over 100,000 events before changing the configurations. This configuration consisted of FED source ids from 50 to 117 inclusive.

We then increased the configuration to 8 crates consisting of fed ids from 50-163 a total of 114 FEDs.

We succeeded to configure the applications but got stuck with the FMM output causing error at the LTC. The source of this problem is understood and tomorrow we hope to go one further and run this configuration.

We had a number of small issues along the way as usual:

1. 3 FED channels were causing problems and no data was being seen in the FRL, it is not known yet if this is FED, transition card or FRL problem.
2. some FED controller pcs had to be rebooted to get the crates to run.
3. the daq had to do something to fix a mapping/routing problem.

Apart from that everything went smoothly.

#### Rack Cooling

It was agreed in the ESSC meeting this week to get an independent expert to evaluate and provide recommendation on the USC55 cooling system.

Meanwhile Oz has continued to experiment with rack cooling (see below). Ivan has also sent him requested heat sink devices and is investigating better alternatives.

> I have installed 7 additional temperature sensors in the middle crate  
> of the rack in the Tracker cubicle. The temperatures are revealing  
> when the sensors are 7cm away from the front panels!

>  
> Slot No. Temperature  
> 2            27  
> 4            40  
> 7            33  
> 10           38  
> 12           29  
> 14           37  
> 16           33

```
> 19          34
>
> I then modified the fan tray (pictures attached) to redirect the air
> flow to the front and have observed a decrease of 4C in the FED
> temperature (the hottest one).
>
> Below are the bin temperatures (sensors 7cm away from the front
> panels) after modifying the fan tray.
>
> Slot No. Temperature
> 2             25
> 4             37
> 7             30
> 10            35
> 12            25
> 14            31
> 16            31
> 19            31
>
> I will start installing the temperature sensors (in slots 4 and 10) to
> the crates in USC55 (as we have done in 904). This will give us a
> better understanding and profiling of the crate and rack temperatures.
```

Oz and Nick has also reported problems with a couple of TIF FEDs tripping due to overtemp during gain scans. The FED settings are not changed during these runs so must be due to changes in light levels. Temp rises of up to 8 degrees were observed during scan. There is some new monitoring software which can track time dependencies of FED temperatures.

### Grounding

Improvements to Rack grounding scheme did not require removing any cards/cables from the FED crates.

### 100 kHz Noise

Further extensive studies at CERN and Imperial have shown that the 100kHz noise effects seen in module tests at CERN are definitely NOT an effect caused by the FEDs.

### **Firmware and Software**

The unpacking speed for the FED event readout has indeed been speeded up by ~ x 6 as previously reported. This was achieved by improving the methods in the offline software. Therefore the proposed Event Format changes which have been implemented and tested in the BE Firmware are not likely to be needed after all.

Problems with DELAY FPGA Fine Skew 64 are now fixed. The “noise” seen during timing calibration runs on some FED channels was due to fitting problems caused by different behaviour of a new version of the tools (ISE 8 removed an output buffer).

Various changes were made to the FE and BE pre-scale logic required by the 100kHz noise tests. Nb APVe addresses recorded by the FED are not guaranteed to be correct when running in pre-scale mode.

**sLHC**

Further CMS UK upgrade meetings have been held at RAL and at CERN. CMS UK have delayed submission of bid to until the December grants committee. The work packages for FE chip and FE FED have now been merged and additional work related to the FE chip power added by the Bristol group. The new doc must be submitted by October 17th.

<b>Actions from the previous PMF</b>			
<b>Action</b>	<b>Status</b>	<b>Who</b>	<b>Original Target date</b>
Fix noise problem with new Delay Fine Skew 64	Done	ST	
Move ORx from bad board to unpopulated Fed.	Done	IC	
Release new VME FPGA document	Done	ST	
Test new heat sinks on ORx	In progress	IC	30-06-07
Merge work package for FED SLHC upgrade.	First Draft Done	JC	

<b>Actions outstanding and new actions</b>		
<b>Action</b>	<b>Who</b>	<b>Target Date</b>
Test 2 newly populated boards.	IC	30-09-07
Test new heat sinks on ORx	IC	31-10-07
Finish final revision of Upgrade Work Package.	JC	10-09-07
Release Draft of Fed User Document	JC	30-11-07
Release 64 bit VME BLT interface ready for board test	ST	30-11-07

**Project Monitor Form- milestones**

<b>Project: CMS FED</b>		<b>PMF number: 68</b>		
<b>Project Manager: J. Coughlan</b>				
<b>Date: Friday 31 August-2007</b>		<b>Sheet: 2 of 2</b>		
	<b>Milestones</b> from <b>Project Management Plan Version:1.6</b>	<b>date due</b> <b>in PMP</b>	<b>predicted</b> <b>date</b>	<b>date</b> <b>done</b>
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off & PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05		28.07.05
33	Production of 500 FEDv3 starts	08.09.05		01.08.05
34	First FEDv3 at B904 Preveessin	30.11.05		27.10.05
35	First FED installed at USC55	17.11.05		19.10.06
36	Last FED installed at USC55	26.07.06		20.07.07
37	Power on Tracker at USC55	01.08.06	01.07.07	
38	Readout test with Tracker at USC55	01.10.06	01.08.07	
39	LHC test run	02.04.07	01.11.07	