Project Monitor Form

Project: CMS FED	**PMF number: 44**
Date: Wednesday 31 March-2004	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Reloading from scratch old set of faulty cards (both returned and undelivered).
A couple of them seem to be working on the test bench.
Still need another week to run through them all.

FEDv1:

Manufacture

All 6 boards are now at RAL and have been boundary scanned (last 2 delivered on 22nd March).
All boards now pass BScan tests (with only minor fixes) except:
Nr 16 had TTCrx errors, nr 15 had QDR errors, but readout tests passed.
2 boards show problems with TTCrx (one is nr 16)
Now testing all analogue channels.
(3 boards had to go back for a few days to have new gain resistors fitted on bottom side).
So far 3 boards look fine on all channels. Remaining problems mostly missing gain resistors (hand soldered).
Nr 13 sent to CERN on 30th March. Could send another board by end of this week.

Readout errors (after some studies localised to BE to VME link) were observed with new cards. Timing in BE FPGA firmware had to be slightly adjusted. Suspect due to changes in line impedance c.f. older cards.
Nb Changed firmware must be used with all new cards, but also works with older cards.
Must also move TTS throttle on J0.
Firmware: ACE 22.03.04 : **Delay 02_1B ; FE 03_15 ; BE 02_39 ; VME 03_0F**

One of the "dud" FED boards nr 09 was examined at National Physical. It was not possible to ascertain further the cause of the FPGA soldering problems without having unsoldered laminate.

FED Status:

Nr 005 at PISA reported some problems inserting card in crate. Not sure which type of crates was used.
Fed nr 003 was checked a few times from RAL and no problems yet observed. Nb it still has very old firmware on it.

System Tests

S-LINK tests based at Imperial .
All remaining problems reported understood as due to artefact of operating scope mode at

excessive rate (as suspected). See below.

RUWG at CERN confirmed that DAQ link cards will handle 80MHz transmission up to 10 metres and that all FEDs are within 10 metres of DAQ cards.

FE FPGA algorithm tests at RAL:
PPD has shown that baseline ZERO SUPPRESSION in FE FPGA is fully working.
Previously reported problems e.g. apparent inability to disable single strips and behaviour of low thresholds, were due to a misunderstanding of input patterns.

Other Tests

Test of over temperature cut out of power. Done.

Tests of Hot Swapping for card extraction and insertion. (requires connection of Front-Panel switch) in progress.
Card extraction working. Card insertion works, but requires an additional push-button reset.
Investigating effect of insertion on other cards in crate.

Power and currents driving all 96 inputs in progress at Imperial. Still in progress. RAL would like to take back nr 06,07 when tests are completed.

Re-confirm at RAL the delay skew settings measured by Matt N.

After re-installation of SBS drivers we are now able to talk to both VME crates from single PC.

FEDv2

Further change review for FEDv2 held at RAL on March 25th.
Agreed on the minimal set of changes (on basis of not changing a working board):
i.e. subset of CALICE power circuit changes (e.g. keep 12V DC-DC device).
Propose reloading VME EPROM via JTAG cable connection on Front-Panel, which can be chained along an entire crate (or more) to a laptop. Slower but less complicated (safer) solution.
Drawing office not ready for layout work until week starting 26th April.
Meanwhile prepare…
Expect the production report from DDi this week. Can then arrange a washout review do discuss possible additional changes for FEDv2.
We plan to have updated FEDv2 schematics prepared.
Aim is to complete FEDv2 layout by beginning of June.
Review and start production of 2 FEDv2 pcbs by end of June for assembled boards in hand August/September.
See project schedule v 1.6

Other Issues

There is now some discussion by CMS ESSC as to whether the “standard” LHC crates/PS provided will be adopted by CMS.

CMS propose to change to single-mode fibres for local TTC transmission. Should be compatible with the existing PIN diodes.

Francois has provided 700 2D bar code labels for FEDs (bags of 100).

Review of FED URD was carried out after last meeting:
The missing features are almost all related to firmware and mostly to do with handling error conditions and resets, which is under development now.

Update of deliverables formalised in Project Spec v2.0

Project web pages have been cleaned up:
http://www.te.rl.ac.uk/esdg/cms-fed/qa_web/index.html

Firmware

Delay-FPGA:
No change. Propose to mask out the 4 “non-linear” of the skew settings in software.

FE-FPGA:
No change.

BE FPGA:

Trigger rule to cure remaining S-LINK readout errors. In Scope mode L1A triggers must be a minimum of 33 clocks apart for BE logic (independent of FE logic rule of SL + 10)

Improvement of state machine for TTS signals implemented (for APVE interface).

Programmed TTCvi card and made a basic test of TTC chan B transmission and serial decoding done.

VME FPGA:

Demonstrated ability to re-load FPGAs under software command and to store more than one set of FPGA configuration files in Cflash card. The set to re-load can be selected by software. Still needs more testing to check reliability of loading.