Project Monitor Form

Project: CMS FED	PMF number: 14
Date: Tuesday 30-April-2002	Sheet: 1 of 2

Project Implementation phase.

News and comment

From now on the minutes and actions of our regular internal design meetings will be formally documented. The PMFs will refer to these documents where appropriate. Accordingly, the frequency of PMFs will be reduced; minimum 1 PMF per month.

On May 14th there will be a review at CERN of FED status (as part of the general CMS electronics week reviews.)

Customer has requested an updated schedule for this review.

Next customer meeting is on 10th May.

Majority of design effort is currently devoted to finalising FE Module schematics (see below.)

Manufacture:

Orders have been placed for VME FPGA and most configuration components.

Quotes have been received for QDR SRAMs.

Order soon to be placed for Elantec Opamp.

Front End Module:

Refer to Design Meeting minutes April 30th for details.

Points of interest:

Aim to have schematics, at rats nest level, of complete FE Module ready for internal review mid May.

All components on FE Module are now chosen and are in Design library.

Final OptoRx pinout is agreed to.

Single stage Elantec Opamp solution chosen.

No indications of problems on bench or in simulation yet, although tests continue. James has the ADC evaluation board modified for Elantec and verified Mark Raymond's basic measurements. He has checked that the ripple seen with AD8138 components is not present with Elantec. Subsequently, it was discovered that perhaps an unlucky choice of capacitors may have caused ripple on AD8138, but there are nevertheless other problems (to do with currents flowing back to OptoRx) observed on AD8138 that are not seen with Elantec.

Opamps will run on +/- 5V (rather than +/- 3.3V).

AD8802 12 channel DAC @ 8 bits for Opamp VREF.

DAC and Temp Monitor will go on reverse side of board.

OptoRx power supply filter is now being simulated with AWB (thanks to Rob's efforts.)

Circa 90% of digital signal pinouts defined by Saeed.

OptoRx spec Doc 020308A, with final pinout, was sent to us from CERN on April 12th.

Additional decoupling located inside OptoRx module does not seem to help noise filtering greatly.

Further information on measurements of the OptoRx signal levels, including the effects of offset controls, have been sent from CERN.

Firmware:
Delay FPGA:
Ed released updated version of documentation and has now started placement in Marcus's group.

Board level:
There is nothing identified at board level which will prevent finalising FE Module schematics.

Updated power estimation for FE FPGA on VirtexII not possible yet due to effort on other projects.

20 x TTCrx ASICs now at RAL.

We still have to identify and order remaining miscellaneous components e.g. connectors, pin diode for TTCrx ..etc

Software:
Proposal for structure of FED online software was presented at CERN tracker meeting 24th April.

Actions from the previous PMF			
Action	**Status**	**Who**	**Target date**
Produce 1st order FE module analogue component layout.	Waiting for schematic with Elantec opamp.	CD/JS	25-02-02
Produce user manual for Delay chip.	Done	EF	
Pass Elantec opamp analogue schematic circuit to Chris.	Done	JS	
Pass details of any remaining components eg DAC to Chris.	Done	JS	
Update FE module analogue layout with Elantec opamp.	In progress	CD	08-05-02
Repeat measurements a la AD devices with Elantec opamp circuit on test board.	In progress	JS	31-05-02
Repeat simulations a la AD devices with Elantec opamp model.	In progress	JS	31-05-02
Identify and obtain quotes on BE components: VME FPGA, QDRAM, EPROM.	Done	JC	

Revise power/current tables for Elantec opamp option.	Done	ST	
Revise power/current tables for FE FPGA in VirtexII model.	Not done	ST/WG	31-05-02
Send analogue circuit diagrams to Francois Vasey.	Done	RH	
Revise power/current tables for FE FPGA in VirtexII model.	Not done	ST/WG	31-05-02

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Update FE module analogue layout with Elantec opamp.	CD	15-04-02
Repeat measurements a la AD devices with Elantec opamp circuit on test board.	JS	15-04-02
Repeat simulations a la AD devices with Elantec opamp model.	JS	15-04-02
Revise FED schedule.	JC/RH	14-05-02
Organise FE Module review.	JC	16-05-02

Project Monitor Form- milestones

Project: CMS FED	PMF number: 14		
Project Manager: R. Halsall **Date:** Tuesday 30-April-2002	**Sheet: 2** **of** 2		
Milestones from **P**roject **M**anagement **P**lan Version**:1.0**	**date due in PMP**	**predicted date**	**date done**
1 User Requirements Document	30-07-01		26-09-01
2 **Project Spec sign off**	**21-12-01**		**05-02-02**
3 Board Level Preliminary Review	14-01-02		16-01-02
4 FE Analogue Channel Feasibility Review	31-01-02		21-03-02
5 FE Module Feasibility Review	28-02-02		30-04-02
7 **Board Level Feasibility Review**	**04-03-02**	**08-04-02**	
8 Delay FPGA Interim Review	31-01-02	04-03-02	
9 Front End FPGA Interim Review	31-01-02	04-03-02	
10 Back End FPGA Interim Review	31-01-02	25-03-02	
11 VME FPGA Feasibility Review	28-02-02	25-03-02	
12 Clock FPGA Feasibility Review	28-02-02	25-03-02	
13 Release Test Plan Document	22-02-02	08-04-02	
14 FE Module Final Review	30-04-02		
15 BE Board Final Review	10-05-02		
16 Full Board Design Final Review	31-05-02		
17 **IDR Customer Production sign off**	**10-06-02**		
18 **Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**26-07-02**		
19 OptoRx for Batch 0 at RAL	26-08-02		
20 **Batch 0 Opto Assembled boards at RAL**	**01-11-02**		
21 Batch 0 review	06-01-03		
22 **Batch 1 (8 off) Assembled boards at RAL**	**21-03-03**		
23 **Delivery Batch 1 to CERN completed.**	**11-07-03**		