Project Monitor Form

Project: CMS FED **Date:** Friday 29-November-2002	**PMF number: 21** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

Schedule:

Now expect Tape out for PCB manufacture by Wed Dec10th.

Slippage due to additional time needed for changes resulting from the internal review and illness.
Now have a task schedule to PCB tapeout which is reviewed daily.
This week was to complete routing.
Next week is to do Power and complete files for production.

This means we will be lucky to get bare PCBs back before Xmas.
Imperial have asked if we can recover time in testing to get one FEDv1 to IC asap.

Personnel:
Ivan Church confirmed to join as Test Engineer.
Starting Dec->Mar @30% and ramping up effort thereafter. Sharing of effort with other projects to be determined.

Staff Effort:

Projections updated. Month by month figures for FYs 02/03 and 03/04. Averaged thereafter.

Manufacture:
Assembly company selected is SAE Tech.
They now have machines for automated BGA assembly (although they may not be used for first pair of FEDv1s).
Parts list has been sent to SAE Tech. They confirmed it as readable. Assembly company SAE Tech preparing for job. Parts list sent. Placement list to do later.
Europractice looking at generation of ODB++ files (in addition to Gerber) for PCB company. Might speed up manufacture.

Problem:
XC2V40 Delay FPGAs : pack marked as ES ie Engineering Samples
Still awaiting confirmation of our part details from supplier. Will chase next week.
Meanwhile checked that clock skew design in XC2V1000 Commercial development board using latest tools works.
Repeated same (again) on XC2V40 ES on development board and it does work.

20x FEDv1:
A few FPGAs already in.
Other parts new quotes are being requested and processed.

Design:
Some late changes (post review).
JTAG chain had to be changed on QDR 2.5 V had to be done.
A few others slipped though.

Went for 14 layer PCB.
Will simplify power planes and allows 2 ground planes.
Implemented changes for impedance matching.

Know changes from review took a bit longer because Cadence still has a few odd behaviours when updating modular design. Therefore had to do some things at board level 8 times over.

BE board. Following critical signals hand routed:
JTAG
FE->BE data and clocks.
BE-FPGA -> QDR
TTCrx clocks; TTS to P0
S-LINK to P2 (differential pairs to accommodate Rob's link scheme in addition to Transition module).
Autorouting of remaining BE signals started.
Improve VME to BE FPGA afterwards if possible.
Tidy up.

Still on schedule to complete routing this week.

Testing:
Delivered PSU for IC. Get backplane in return from IC.

Electrical only test boards proposed..

I) Transformer. Simple. Basic tests
II) Electronic with DAC. Demanding. Advanced tests.

I) proved difficult to fit in layout.
II) can't afford design effort (given that this card will only be used on FEDv1s whilst they don't have OptoRx placed and we have to finally verify FEDv1 with the OptoRxs).

Propose we go for an intermediate design.
III) Cross point switch plus AD8131 Opamps (see James's slides).

Intend to drive by Signal Generator or ARB but…
But would it also be possible to use IC board to drive FED electrical inputs (i.e. post OptoRx).? Is it worth investigating?

Thinking about simple test designs needed to get going. Eg clock distribution.
New Test Engineer (Ivan Church) starting Dec could assist with this.

Firmware & Software:
VME-FPGA:

Write engine sending serial stream to FE FPGAs (via BE FPGA) working.
Read engine in progress.

Now trying to install Laurent's Tracker DAQ packages.
Another Online S/W meeting next week.

DAQ:

Next RUWG: CRC design for S-LINK data checking.

DAQ link implementation. Replied to Attila, but discussion may continue during CMS week.

AOB:
Fibre-Optic Safety Course confirmed for RAL for Friday 20th December (morning).

In future PMFs will serve as Customer meeting reports.
All of the Project web pages will be made accessible to outside access. This will avoid duplication of reports and files and reduce effort involved in QA maintenance.

Next Meetings:

CMS week 49. Online S/W meeting. RUWG.
FED-UK Meeting Friday 13th Dec 10:00 at RAL.

Actions from the previous PMF

Action	Status	Who	Original Target date
Board level routing completed.	Done	CD	
Tape out to PCB manufacture.		CD	15-11-02
Produce FED software driver lib API.		JC	29-11-02
Order DAQ PC.		PPD	06-12-02
Re-Test Delay FPGA design on XC2V1000C board	Done	EF	

Actions outstanding and new actions

Action	Who	Target Date
FED sign off and out to manufacture.	CD	11-12-02
Produce FED software driver lib API.	JC	13-12-02
Order DAQ PC	PPD	06-12-02
FED board ready for internal Design Office check	CD	03-12-02
Tape out to PCB manufacturer	CD	11-12-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 21**		
Project Manager: J. Coughlan **Date:** Friday-29-November-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02	30.08.02	
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off&Board Out**	**07.10.02**	**11.12.02**	
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**	**24.01.03**	
18	OptoRx for Batch 0 in UK	26.08.02	06.01.03	
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		