Project Monitor Form

Project: CMS FED **Date:** Thur 29 Sept-2005	**PMF number: 57** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

Progress is good. We are slightly ahead of the predicted FED delivery profile shown at last Tracker week (see below).
Now expect to start with delivery to CERN of ~35+ boards in October.

Our special FED Test setups were prepared and fully installed at the Assembly plant in July/August. Their staff were trained by our engineer and are now routinely running the tests, although with some expert assistance from our engineer on request.

The Test bench is working well. Ivan has made a few trips to Calne to help with less obvious problem boards and to pass feedback on minor snags on received boards.

The 1st batch of 50 FED boards was manufactured as planned in August.
(first 2 boards were assembled and tested in late July to verify production).
48 have so far passed the Assembly plant tests.
A couple have persistent Bscan problems and will need some rework.

One minor patch to –12V monitor LED has been found necessary.

After some oven tests with dummy modules it was decided by eXception engineers to continue with conventional assembly of ORx modules rather than SMT. It was not found possible to keep within parameters of the solder paste. In addition, they had concerns that ORx could be damaged in subsequent conventional assembly steps as they protrude from the board.

The 2nd batch of 50 boards is now being assembled and some are under test at Calne.

42 of the passed boards are at RAL
38 of these have now passed our additional tests (ORx input testing, TTC and SLINK).
4 have some problems, which we are investigating. But there are no common faults yet.
A further 12 have been dispatched to us.

Results of tests are being archived and backup of disks at Assembly Test bench are being made.
Board status is recorded in a production summary spreadsheet.

A short document has been produced summarizing the Acceptance tests to be carried out at RAL. The tests are based on a selection of James' Test suite.
As requested all boards will in addition also be powered overnight.

Our general policy is to put any boards failing tests to one side and go back to them after testing the whole batch. If we spot a systematic failure we would halt production.

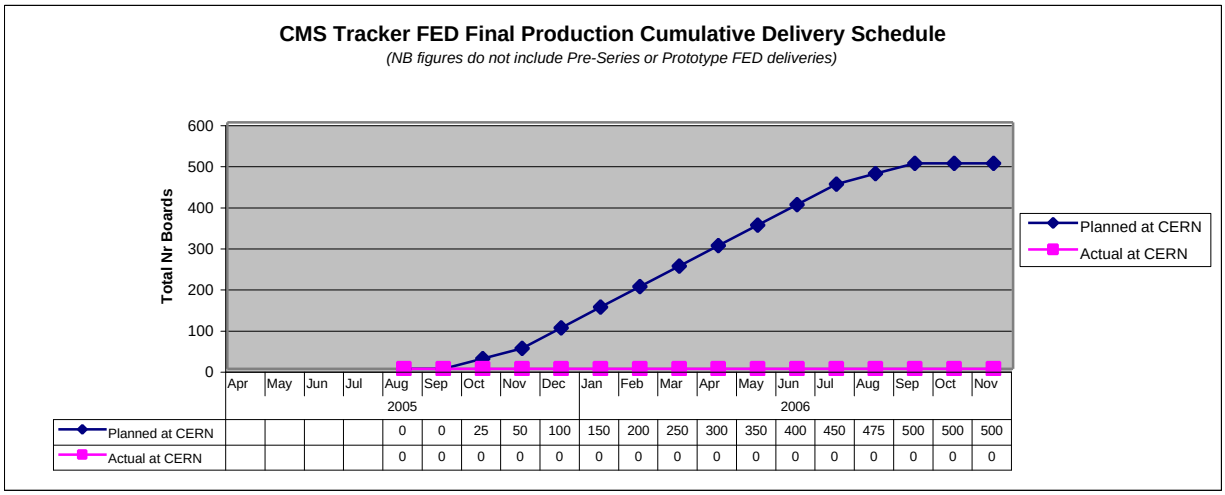
Our plan is to continue with tests of the production boards during next 2 weeks.

We would aim to ship between 30 - 40 boards early week of Oct 17th.
They should then be there during Tracker week.

Production boards should not be used in Assembly centers.

Meanwhile, for Assembly center needs, we will retest and if ok, send ~ 4 of remaining v2 pre-series asap.

About 150 production boards will be needed for Full Tracker surface tests in B186.



	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov
					2005										2006					
Planned at CERN					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
Actual at CERN					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Production Concerns:

The lead time for the SYSTEM ACE controller (FPGA configuration) has increased ~ 20 weeks? due to disruption at Xilinx fab. We had enough for 125 boards in total. We are investigating obtaining from alternative sources.

Transition Card

70 cards have been manufactured (using Imperial design files) and all tested ok.

35 of these are now at B904.

Once cards have been verified with final DAQ SLINK system we will place order for remaining 400.

BOM needs minor additions before next production.

Firmware :

VME FPGA:

The problems with VME Block Transfers with both CAEN and SBS are ‘fixed’ (no problems have yet been reported from CERN or LSA systems).

The SBS BLT read problems, which only showed up in certain crate configurations and was therefore difficult to debug, was traced to a race condition between DTACK and DATA out.

There is still a driver problem with dual processor PCs and CAEN. And possibly with SBS?

The BLT32 readout speed has also now been considerably improved with relatively minor changes to the logic:

Originally (e.g. Lyon DAQ tests) : ~ 6 MB/s
Step 1 : Reduced data path in BLT logic => ~ 9 MB/s
Step 2 : Speeded up internal clocking => ~13 MB/s

These results are in agreement with measurements made at RAL and by Oz and Costas.

Measuring with a commercial memory card shows limit of ~16-18 MB/s with SBS or CAEN Depending on PCI card arrangement.

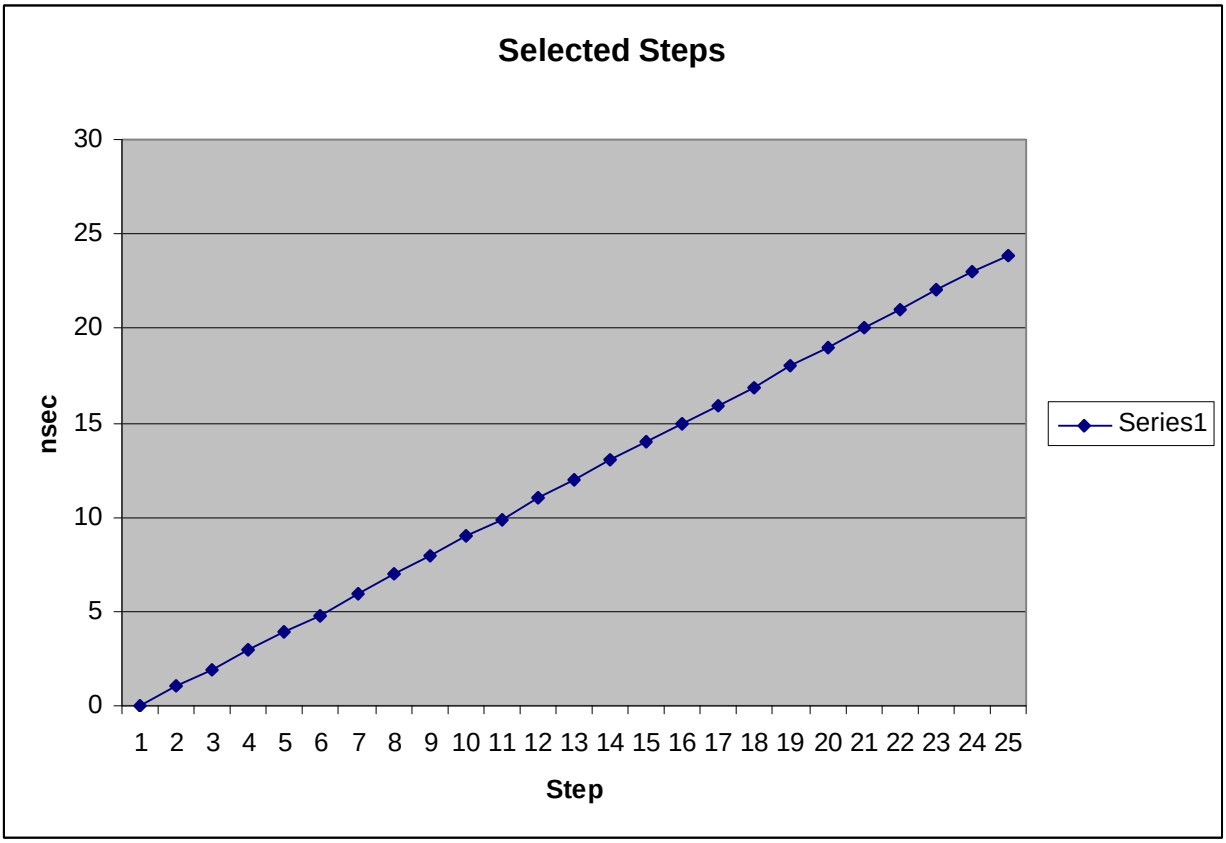
To reach this limit with FED would need to introduce a Pre-Fetch mechanism, which is a more major change.

To go beyond this will need to implement MBLT64 (approx doubling of rate).
The SBS can't operate in this mode but the CAEN datasheet says it can.

DELAY FPGA:

Work has been done to remove the existing discontinuities in the fine skew coverage.
By increasing the internal number of fine DCM steps to 64 we can provide a smooth evenly spaced set of 25 x 1 nsec steps.

This will only require a change in the final low level software, but it will NOT be backward compatible with earlier firmware releases.



FE FPGA:

Further tests with Fake Frame generator have been made with debug software. Final software is needed for use in Tracker DAQ.

ZS-Lite mode (reduced data) has been implemented and some basic tests carried out with debug software. Event data appears correct. Contents of header are still being investigated.
Presently the median and codes are removed, but the lengths remain in bytes. To go to absolute minimum data with cluster count will require more major changes.

Selection of the bits to remove when going from 10 bit to 8 bit data has been implemented, but not tested yet.

The VHDL version with all these improvements has to be thoroughly tested with Final Software and Tracker DAQ before it can be released as a new standard.

REMAINING FIRMWARE & SOFTWARE REQUIREMENTS:

Spy Channel in Frame Finding mode: Needs work in both FE and Delay

Data Buffer Overflow Recovery: Needs work in both FE and BE

Need Final Software to support many new features introduced in past 6 months….

PPD have recruited a new RA.

A document describing the Event Format (based on BE and FE technical descriptions) has been released.

Equipment

3 VME bus extender boards were ordered and expected soon.

TTCoc box Front Panels are now at RAL.

As CERN stores are too slow, an alternative source (in UK) has been found for TTC fibres and couplers.

Oz is organizing equipment for B904.

Other Activities:

RAL rack water cooling was installed last week and it is now up and running.
Ivan is improving the sealing of the racks and is making tests with the Rack turbine.
Board temperature measurements are being repeated to find an optimal slot arrangements.
However, these tests will need to be finalised using Racks in B904.
Some nice display software e.g. Labview would be helpful here.

A firmware module is being introduced which will initialise the Tcrit shutdown temperature at FED power up (as a fail safe).

Safety Training at CERN needs to be done before end of year (for underground access etc).

Agreement with CERN was finally signed in August.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Fix remaining pre-series boards and send to CERN.	In progress	IC	30-06-05
Get Test kit running at Assembly plant.	Done	IC	
Fix Block Transfer firmware.	Done. Also speeded up.	ST	
Test ZS lite firmware.	In progress.	JC	31-07-05

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Fix remaining pre-series boards and send to CERN.	IC	07-10-05
Test ZS lite firmware.	JC	31-10-05
Test 10 bit to 8 bit FE firmware.	JC	28-10-05
Update Transition Card BOM.	ST	28-10-05
Have first batch of production FEDs ready for delivery to CERN.	IC	17-10-05
Implement Firmware for automatic TCRIT shutdown.	ST	28-10-05
Order TTC fibres and couplers.	IC	28-10-05
Attend CERN Safety Training	IC, JC, ST	28-10-05
Optimise FED slot arrangement in cooled rack.	IC	28-10-05
Summarise FED Finances.	JC	28-10-05

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 57**		
Project Manager: J. Coughlan **Date:** Thur 29 Sept-2005		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05	22.07.05	28.07.05
33	Production of 500 FEDv3 starts	08.09.05	27.07.05	01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05	30.10.05	
35	First FED installed at USC55	17.11.05	01.03.06	
36	Last FED installed at USC55	26.07.06	31.09.06	
37	Power on Tracker	01.08.06		
38	Readout test with Tracker	01.10.06		
39	LHC test run	02.04.07		