Project Monitor Form

Project: CMS FED **Date:** Tuesday 29 June-2004	**PMF number: 47** **Sheet:** 1 **of** 2

Project Implementation phase.

PMCs:
Final spreadsheet updated. Summary of spares. Test bench is being dismantled.

FEDv1:

Two more boards (nrs 15 & 16) were shipped to CERN on 25th May. All known patches (eg for S-LINK) applied.

Board nr 12 with new QDR memories reworked came back during CMS week. Job was delayed as a new frame (to accommodate connectors) had to be made to hold board flat during rework. QDRs have been tested with VME readout of events (although set-up wasn't operational to do Bscan tests). Propose to purchase production quantities of these parts.
Nb they will not be available in time for first 2 FEDv2 so will place old QDRs on these.

FEDv2

Final review of FEDv2 design was held on June 4th. Only very minor alterations necessary since previous review. The majority of the layout suggestions from DDi were carried out.
Component kit ready (just need OptoRx).
Updated quotes based on final files were obtained after a slight delay and job was sent out on June 28th as planned.
Expect 2 assembled boards back in second half of August.

Other Items

10 more FEDv1 Front Panels now in hand. Jan Troska later requested increasing OptoRx holes for bar codes. Will be modified and sent this week.
50 more blanks for FEDv2 available. Lettering for LEDs is finalised. FE FPGA modules will now be labelled from 1 to 8 (bottom to top) as agreed for new channel numbering scheme.

Firmware :
Measurements of VME Block readout speed with VME bus analyser confirm behaviour of SBS drivers and rates (6 Mbytes/sec) measured at CERN and are in agreement with subsequent measurements by Costas with a CAEN (USB) interface. With SBS the FED accounts for 70% of total Block Transfer read time of 600 nsec. Looking at steps to speed up this part of firmware.

Verified that serial write commands can be chained together. This means that the pedestal data can be loaded taking advantage of Block Transfer speeds.

SystemACE Compact Flash card reading and loading from VME is no longer working. Firmware hasn't changed?

List of missing features from FED firmware released by Ian on 23rd June.

Draft Technical Description of BE FPGA design released.

Testing :
A draft specification for testing at the Assembly company was discussed at this meeting.
A pcb card on J0 backplane to chain programming of VME EPROMs is being laid out.
Summary of assembly faults from last batch made.

FED Tester card at RAL will be exchanged for new version of board today.

CERN may offer to give/loan us a water-cooled rack? Required for full crate tests.

Tender :
First part of department EU Framework Tender is complete. FEDv2 design will be used as one of the examples for 2nd stage to start in next couple of weeks.

Test Beam 25 nsec :
4 FEDs were used in readout (2 were equipped with S-LINK during 25 nsec run).
FEDs were installed quickly and worked well during tests.
Some problems nevertheless:
- Learnt that disabling unconnected fibres only worked by setting cluster thresholds appropriately.
- Corruption of event formatting for some events was observed (only) in Zero Suppression mode. Trying to reproduce these errors at RAL with FED Tester inputs.
- Possible loss of synchronisation between FEDs was suspected, but no evidence of problem (eg FED counter values) received yet.
Fuller report to come at this meeting.

Transition card schematics from James Leaver (Imperial) examined. Only very minor suggestions (eg add leds) made.