Project Monitor Form

Project: CMS FED	**PMF number: 31**
Date: Thursday 29-May-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Intensive efforts were made to complete as many PMCs as possible before test engineer left.
We now have almost 30 (of 40) cards passing all our test procedures.
These cards are just waiting for Front Panels before delivery. There were unexpected problems with the company redoing the lettering. FPs are now expected next week.

Rough summary of test results from 40 cards:
(Nb all cards have had patch for flash eprom power as discussed in last report.)
23 cards were "perfect"
A further 6 had relatively simple to spot problems (resistor missing or wrong value) and have been fixed.
11 have less obvious, but varying, symptoms and were put to the side. Hopefully, given time most of these can also be cured.

On a positive note, none of the cards so far tested exhibit the intermittent booting problems seen from the 2001 production.

Jonathan Godwin actually leaves RAL today for 6 months duty in Iraq. 9U FED engineer Ivan Church has been trained and will take over remaining PMC testing.

Further efforts have also been made to verify location and status of cards from previous production runs.

FEDv1:

Manufacture

3 PCBs went out to assembly company on 19th May as planned.

Updated quotes obtained for FEDv1 Assembly and larger FPGAs.
Assembly : 10-20 off £2,000
50 off £1,500
100 off+ £,1000 (approximate figures)

XC2V1500 (200 off) is now £150 (cf £167 6 months ago.)
XC2V2000 is now £213 cf £242

A request has also been made to distributor for longer term price forecasts for our Xilinx FPGAs.

Firmware

Progress has been slower than hoped.

FE-FPGA:
Ivan continues testing Bill Gannon's final design.
In Scope mode we can now see data on all 12 fibres. Previously had seen only 6 fibres as ChipScope was running at 40MHz whereas data is output at 80 MHz. Headers and data for first 11 fibres appear correct (Nb all data should be 0 as no input signals.). But data in last fibre is corrupt. Now investigating if it could be caused by a timing problem.
Some of Ivan's time was diverted to PMC training (see above.)

BE FPGA:
No progress to report as Saeed only returned from sick leave today.

VME FPGA:
Serial read-back of FE registers is still only partially working. The behaviour is quite hard to understand. Ed Freeman is continuing tests. Nb we have never observed any problems when loading these registers.
Matt N. has reported a bug in FED driving some signals eg DTACK, which could sometimes cause conflicts when other slaves are in the crate. It should be straightforward to fix.

Software
Matthew P. has written a test program to configure and read-back about half of the possible register types in the Front End FPGA. This is expected to replace John's original hacked code in order to test VME firmware.
Fed API. A basic interface class sitting on top of Matthew's low level classes is close to being ready.

Other Tests
Temperature measurements (with IR thermometer) show FE chips eg ADCs and Delay FPGAs running (very roughly)
45 degrees C (at top) ; 48 (in middle) ; 50 (at bottom). Nb Fan is at Top of our crate.

Total current measurements indicate we may be higher than expected on 3.3V supply at 13 A which is close to maximum of 15 A. Measurements need repeating when all final designs are operating with real data flow through FPGAs.

As part of work on another project, Rob is testing the Xilinx reference design for Channel Link implementation on Virtex-II development board. This is proposed as replacement for DAQ PMC card S-LINK implementation.