

Project Monitor Form

Project: CMS FED Date: Thursday 29-May-2003	PMF number: 31 Sheet: 1 of 2
<p>Project Implementation phase.</p> <p><i>FED-PMCs:</i> Intensive efforts were made to complete as many PMCs as possible before test engineer left. We now have almost 30 (of 40) cards passing all our test procedures. These cards are just waiting for Front Panels before delivery. There were unexpected problems with the company redoing the lettering. FPs are now expected next week.</p> <p>Rough summary of test results from 40 cards: (Nb all cards have had patch for flash eeprom power as discussed in last report.) 23 cards were “perfect” A further 6 had relatively simple to spot problems (resistor missing or wrong value) and have been fixed. 11 have less obvious, but varying, symptoms and were put to the side. Hopefully, given time most of these can also be cured.</p> <p>On a positive note, none of the cards so far tested exhibit the intermittent booting problems seen from the 2001 production.</p> <p>Jonathan Godwin actually leaves RAL today for 6 months duty in Iraq. 9U FED engineer Ivan Church has been trained and will take over remaining PMC testing.</p> <p>Further efforts have also been made to verify location and status of cards from previous production runs.</p> <p><i>FEDv1:</i></p> <p><u>Manufacture</u> 3 PCBs went out to assembly company on 19th May as planned.</p> <p>Updated quotes obtained for FEDv1 Assembly and larger FPGAs. Assembly : 10-20 off £2,000 50 off £1,500 100 off+ £,1000 (approximate figures)</p> <p>XC2V1500 (200 off) is now £150 (cf £167 6 months ago.) XC2V2000 is now £213 cf £242</p> <p>A request has also been made to distributor for longer term price forecasts for our Xilinx FPGAs.</p> <p><u>Firmware</u></p> <p>Progress has been slower than hoped.</p>	

FE-FPGA:

Ivan continues testing Bill Gannon's final design.

In Scope mode we can now see data on all 12 fibres. Previously had seen only 6 fibres as ChipScope was running at 40MHz whereas data is output at 80 MHz. Headers and data for first 11 fibres appear correct (Nb all data should be 0 as no input signals.). But data in last fibre is corrupt. Now investigating if it could be caused by a timing problem. Some of Ivan's time was diverted to PMC training (see above.)

BE FPGA:

No progress to report as Saeed only returned from sick leave today.

VME FPGA:

Serial read-back of FE registers is still only partially working. The behaviour is quite hard to understand. Ed Freeman is continuing tests. Nb we have never observed any problems when loading these registers.

Matt N. has reported a bug in FED driving some signals eg DTACK, which could sometimes cause conflicts when other slaves are in the crate. It should be straightforward to fix.

Software

Matthew P. has written a test program to configure and read-back about half of the possible register types in the Front End FPGA. This is expected to replace John's original hacked code in order to test VME firmware.

Fed API. A basic interface class sitting on top of Matthew's low level classes is close to being ready.

Other Tests

Temperature measurements (with IR thermometer) show FE chips eg ADCs and Delay FPGAs running (very roughly)

45 degrees C (at top) ; 48 (in middle) ; 50 (at bottom). Nb Fan is at Top of our crate.

Total current measurements indicate we may be higher than expected on 3.3V supply at 13 A which is close to maximum of 15 A. Measurements need repeating when all final designs are operating with real data flow through FPGAs.

As part of work on another project, Rob is testing the Xilinx reference design for Channel Link implementation on Virtex-II development board. This is proposed as replacement for DAQ PMC card S-LINK implementation.

Actions from the previous PMF			
Action	Status	Who	Original Target date
Produce FED software driver lib API.		JC	29-11-02
Test FE to BE FPGA and QDR data write path.		IC/ST	04-04-03
Send first batch of FED-PMCs to CERN.		JG/JC	09-05-03

Actions outstanding and new actions		
Action	Who	Target Date
Produce FED software driver lib API.	JC	06-06-03
Test read-back of FE.	EF/JC	13-06-03
Test FE to BE FPGA and QDR data write path.	IC/ST	13-06-03
Send first batch of FED-PMCs to CERN.	JG/JC	13-06-03

Project Monitor Form- milestones

Project: CMS FED		PMF number: 31		
Project Manager: J. Coughlan				
Date: Thursday 29-May-2003		Sheet: 2 of 2		
	Milestones from Project Management Plan Version:1.3	date due in PMP	predicted date	date done
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off & PCB Tape Out	07.10.02		06.12.02
17	Batch 0 (2 off) Non-Opto Assembled boards at RAL	11.11.02		22.01.03
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	Batch 1 (10 off) Assembled boards at RAL	04.07.03		
22	Delivery Batch 1 to CERN start	12.09.03		
23	Delivery Batch 1 to CERN completed.	04.12.03		