Project Monitor Form

Project: CMS FED	**PMF number: 29**
Date: Tuesday 29-April-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

20 assembled PMCs at RAL.
Missing inductors have held up remaining cards. Now gone to new distributor and expect inductors next week.
Set up the PMC test bench (took back NI/VXI interconnect from FED crate.)
We started testing first 5 cards. Preliminary loading and input tests ok.
Measurements with internal clocks and triggers showed up 2 bad channels (out of 40). One was loose resistor (easily located and fixed). Second (gain setting off) is now looked at.
Meanwhile we found a major problem. Cards would not boot FPGA from Flash EPROM.
But found that replacement Atmel Flash (AT45DB041B) part had been provided which now expects Vcc =.3 V cf 5V. NB Basic tests including read/write to Flash memory appeared ok.
Fortunately can patch this on board. (and signal inputs were still compatible with CPLD.)
Now all patched cards boot reliably.
Setting up for external clock and trigger tests.
Few more minor tests to do then load final firmware version and test in Linux PC before delivery.

FEDv1:

<u>Electrical Testing</u>
James has been testing driving >1 FE modules at once by chaining N test cards together driven by one signal generator. Found (and fixed) 1 bad channel on FEDv2 (dry joint on diode.)
Intention is to use this with final firmware to get some realistic power measurements (albeit without OptoRx.)
Improved user manual for test card.

<u>Firmware</u>
Upgraded tools. To FPGA Advantage 5.4 and Xilinx 5.2
Cures System ACE file creation problems (can now have > 30 FPGAs on chain).

Delay FPGA: Final design is now in standard load (i.e. in Compact Flash.)

FE-FPGA: Ivan has taken Bill Gannon's source design and produced bit file. Added chip scope on input channels.
Tested DDR data transfer from Delay to FE FPGA works.
Now in standard load.
Next test using Scope Mode readout. Need serial comms or fix registers.

BE FPGA: Close to being ready to test. Several blocks implemented despite problems caused by tools upgrade. Tracker header information from FEs now added. Data path for readout to VME is implemented (with necessary hold offs for VME FPGA buffers.)
Now doing final timing simulations. Still have a problem with circuit for responding to buffer

overflows (will skip this logic if necessary and just ensure no overflow conditions can occur.)
Need some minor additions for Scope Mode (add software trigger register and dummy tracker header.)
Aim to produce bit file this week as Saeed is effectively then off for 2(3) weeks.
Ed/Ivan can add serial comms receiver and Chip Scope to test data transfers.

VME-FPGA: Serial comms sender in VME FPGA is working. Problem in receiver in BE FPGA is being debugged. Some bugs were introduced to basic VME interface, but were later cured.

CERN Tracker Week
New FEC system will use QPLL chip in clock chain. Requires new TTCvi when using new FEC.
But no changes needed to FEDv1.

Requirements for functionality (firmware and software) of FEDv1 in Large Scale Assembly centres were clarified.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Produce FED software driver lib API.		JC	29-11-02
Get OptoTest card bench working at RAL.	Done	MN	
Test serial comms between VME and BE FPGA.		EF/JC	28-03-03
Test FE to BE FPGA and QDR data write path.		IC/ST	04-04-03

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Produce FED software driver lib API.	JC	30-05-03
Test serial comms between VME and BE FPGA.	EF/JC	02-05-03
Test FE to BE FPGA and QDR data write path.	IC/ST	02-05-03
Send first batch of FED-PMCs to CERN..	JG/JC	09-05-03

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** J. Coughlan **Date:** Tuesday 29-April-2003		**PMF number: 29** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off &PCB Tape Out**	**07.10.02**		**06.12.02**
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**		**22.01.03**
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		