Project Monitor Form

Project: CMS FED **Date:** Monday 28-January-2002	**PMF number: 06** **Sheet:** 1 **of** 2

News and comment
Feasibility Study continues.

Front End Module:
Chris has received schematic from James. Schematic needs slight mods to adhere to BS standards as used by DO. Chris will show James how this is done. James also has a few minor simplifications to existing circuit.
Simulation work is progressing. In particular work on PS filter circuits for OptoRx. PSRR is specified at only 20dB at 1MHz.
Rob will enquire whether we can use license for Simulation tools for use on James's PC.
Chris would like more information on power supplies to OptoRx.
Adam has comments on OptoRx pin arrangement and may provide suggestions for improvements.

Firmware:
Ed's chip was reviewed at last week's design meeting. The user I/O pin availability is quite tight. However he now has a solution for covering 360 degrees phase shift on all 4 DCMs. Ed will try and implement this next. He will also prepare a realistic preliminary pin out for FE module layout work. Tests of the feasibility of DCI and DDR features used in the design are also required. Ed is due to start a 6 month placement in MicroElectronics in April.

Board level:
Adam and Saeed have discussed board level design tasks. Saeed will start to work on board level design eg clock chain, boundary scan chain.

Other issues:
Customer has asked us urgently to investigate how much we can spend this financial year on components for up to 10 FEDs. A preliminary procurement list has been produced. Possible candidates for spend this FY are ADCs and XC2V2000 FPGAs.

Notes:
Actions include those resulting from FED design meeting.

Actions from the previous PMF

Action	Status	Who	Target date
Produce procurement list for 9U Prototype	Done	JC	
Investigate tools to create CADENCE symbols of Xilinx FPGA.	Ongoing	RH	21-01-02
Pass schematic for Analogue part of Front End module to DO	Done	JS/CD	
Test key aspects of Delay FPGA on development board in Lab	In progress	EF/RH	31-01-02

Put LHC crate info on web	Done	JC	
Link VITA specs to web	Done	JC	
Obtain estimate for manufacture 500 H1FTT as guide of CMS costs.	In progress	BT/CD	18-02-02
Specify board level voltage and current requirements.	In progress	ST	18-02-02

Actions outstanding and new actions

Action	Who	Target Date
Pass component details for purchases this FY to Bob T.	JC	04-02-02
Investigate tools to create CADENCE symbols of Xilinx FPGA.	RH	04-02-02
Test key aspects of Delay FPGA on development board in Lab	EF/RH	31-02-02
Produce preliminary pinout of Delay FPGA.	EF	11-02-02
Obtain estimate for manufacture 500 H1FTT as guide of CMS costs.	BT/CD	18-02-02
Investigate temperature monitoring of FE Module (OptoRx/Virtex)	JS	28-02-02
Book cards (9U FED/Test cards) into Drawing Office	JC/RH	28-02-02
Specify board level voltage and current requirements.	ST	18-02-02
Add members to cmsfed unix group for web access.	JC	04-02-02
Produce proposal for web pages reorganisation	AB	04-02-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 06**		
Project Manager: R. Halsall **Date:** Monday 28-January-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01	31-01-02	
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	31-01-02	
5	FE Module Feasibility Review	28-02-02	28-02-02	
7	Board Level Feasibility Review	04-03-02	04-03-02	
8	Delay FPGA Feasibility Review	31-01-02	31-01-02	
9	Front End FPGA Feasibility Review	31-01-02	31-01-02	
10	Back End FPGA Feasibility Review	31-01-02	31-01-02	
11	VME FPGA Feasibility Review	28-02-02	28-02-02	
12	Clock FPGA Feasibility Review	28-02-02	28-02-02	
13	Release Test Plan Document	22-02-02	22-02-02	