Project Monitor Form

Project: CMS FED	**PMF number: 38**
Date: Monday 27 October-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Re problem from last report.
One batch of 20 PMCs ser nr 90-109 had incorrect resistors on output of Voffset to Opamps. Two resistors per card.4K7 fitted instead of 4R7.
Effect of fault was to couple input signal on one channel to other channels. Fault does not show up on simple Voltage measurement test. Need to reinstall PMC test bench to verify if any effect would show up on sine wave test. This was already planned in order to complete tests of remaining PMCs.

14 from faulty batch were sent to CERN (unfortunately 3 are already in USA.).
Remaining 11 were returned to RAL for resistor replacement. They were sent back to CERN on Oct 24th. Resistors also replaced on un-shipped PMCs.

PMC test bench is being set up again to complete delivery of remaining cards.

FEDv1:

Manufacture

6 FEDv1's came back from assembly on Oct 8th as expected.
Visual inspection looked good. First board modified and problems discovered on power up. Shorts between 3.3V and Gnd then found on all 6 boards. Shorts between 1.5V and Gnd on 4 of boards.

Express circuits say 7 pcbs were made of which 1 failed bare board tests.
They are sending summary of test results for remaining 6 which passed bare board tests.
These boards are the first FEDs manufactured with the immersion tin finish (cf gold on previous.) Apart from that there were no changes in design.
The tin finish is meant to ensure improved lifetime stability of soldering.

Assembly company SAETech took one board back for closer X-ray inspection.

Last week one FED had all 9 large (676 pin) FPGAs removed. The pcb was cleaned up and brought to RAL for inspection.
It appeared that on a number of pads there had been no solder. This solder had then migrated to other pins causing shorts.
The prime suspect remains a contamination of the finish on the PCB and is still under investigation. Note that contamination was also seen using Gold finish on earlier Atlas boards.

The board was sent back and new FPGAs were put down (this process involves removing and refitting some other parts, notably OptoRx modules).

The board was powered on the bench successfully. ie shorts are repaired.
Boundary Scan tests have shown about 10 connection errors restricted to 2 of 24 Delay FPGAs (almost all on one of them.)
This will mean replacing these 2 small FPGAs.

We also have to anticipate potential problems with digital connections from FPGAs to the analogue inputs, which we won't see until we inject data on the board.
These tests have now begun.

A second FED is now in process of repair at assembly company.
Based on these 2 boards we will decide if it is worth proceeding with other 4.

Removed FPGAs could be recovered by re-balling, but cost needs verifying to see if it's worthwhile.

Delivery:
Milestone to deliver first FED nr 005 to CERN by end of October, followed by second in November.
First board 005 has been checked out with "ramp" data from OptoTester and root display software. All 96 channels look ok. All digital functions check out ok including TTCrx.
For second board Nr003 on loan to CALICE has been taken back and assembled with new OptoRx. Needs data checking on all channels and TTCrx BScan.
Juggling FEDs… Nr 004 (was being used for power tests) was brought into a fit state for CALICE to use.
NB CALICE pcbs are out on 10 day turnaround (with new pcb manufacture but same assembly company.)

Ivan is looking at changes involved to modify 005 for 1V pp operation. Perhaps 1 day to change and test.

System Tests
SBS VME interface installed in lab crate. All programs now operating with SBS.
9U FED OptoTester brought to RAL on Oct 9th.
Final software had few bugs uncovered during these tests. Now working well.
Improvements to OptoTester software and display very helpful.
Further improvements already suggested, which would aid testing considerably.
1. Display of all 12 FE channels at once.
2. Automatic checking of event formats, header structures, summaries of synchronisation status bits.

Verified Scope mode operation.
Verified Frame Finding operation. Timing scan neatly shows frame finding synchronisation (data readout in tracker header) behaving as expected. Need also to be careful not to disable apvs and to set frame thresholds appropriately on all channels.
Verified clock skewing on all channels.

TTC tests with TTCvi (MkI) and TTCvx cards (refer to last report):
Using FED 005 TTC clock and triggers have been successfully sent using both old TTCvi /

TTCvx and new TTCvi(MkII) / TTCex pairs.
Possible reasons why so many previous problems getting system going: FED 002 TTCrx needs checking, duff lemo cable(s), order of connection of lemos and powering of TTC cards matters! But we do now have a working TTC generator system. IC TTC cards can be returned.

But still have FEDs with TTCrx powering up in an unusable state.
We now have a BSDL file for TTCrx (file wasn't available last time we requested.) Put back TTCrx on JTAG chain and retest existing FEDs.

Analogue Tests

Further measurements on ADC9218 development board at Imperial show size of pre-pulse undershoot effect is proportional to input pulse height.
Pre-pulse undershoot effects are also present on 105 MHz speed grade device (also implies effects not batch related as we use 65 MHz grade.)
But effect is not present when ADC is put in 1V peak to peak mode. We were operating in 2V peak to peak mode to match expected OptoRx output range.

Analogue Devices technical experts are now actively investigating these effects. They may have a possible explanation:

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"The input sampling mechanism is different in the two modes; in 1Vpp mode a
sampling cap in the input pipeline is cleared between samples as part of the
track/hold process. in 2Vpp mode, this 'clearing' of the sampling cap does
not occur, but is carried thru the pipeline.  This indicates a potential
sensitivity in 2Vpp mode for a pulse-type sampling application."
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Matt is trying 2 solutions on some FED channels to match 1 Vpp range (i.e. to reduce gain by 1/2.)
a) Reduce sense resistor on OptoRx output from 100 to 50 Ohms (advantage no layout changes).
b) Add 100 Ohm terminating resistor across outputs of OpAmp.

Other Issues
LHC crates (3 off) were finally shipped from CERN on Oct 10th. At time of meeting still hadn't arrived at RAL. Shipment may have been addressed to ATLAS?

Strengthening bars have been made and are now being fitted to FEDs.

Production Manufacture

Meeting held on Oct 6th with Procurement Officer rep for INS, Lindsay Glover.
Recommendation is to follow Restricted OJE procedures (OJE mandatory for sums over ~£150K). This takes slightly longer, but includes a market survey stage before the tender proper during which the companies that will be allowed to tender can be chosen.
Lindsay will provide some example documents from previous projects going through OJE procedures (Diamond.)
CMS tracker institutes appear agreeable to UK handling all aspects of procurement and manufacture.
FED procurement committee to be formed with representatives of all stakeholders on project.

A general EU contract for PCB Manufacture, Assembly etc for future INS projects has recently been drawn up by Viraj Perera INS Electronics System Support group leader. The requirements should fit FED needs. A list of manufacturers has been drawn up.
A visit to one of them will be arranged very soon.

Firmware

Firmware that can be used for Large Scale Assembly tests is now Ready.

Delay-FPGA:

Odd effect in serial command interface causing every second command to be ignored. Thought to be caused by spurious bits coming after end of serial command. Solution in software is to clear memory location after location holding command word. Believed to only affect serial commands that are passed through from FE to Delay FPGA.
System tests verified coarse and fine skewing working on all 4 FPGA delay channels version Delay_02_15 using Debug software. Important now to test with Final software.
Ed is doing final tuning measurements of fine skews.

FE-FPGA:

Saeed has taken over design from Ivan.
Full I2C interface to LM82 Temp sensor implemented in firmware. Temperature monitoring and software trips tested with Debug software. Hardware trips not tested yet.
Full serial interfaces to TrimDACs implemented in firmware and tested with Debug software. Software interfaces are now much simpler. Final software still to be implemented.

BE FPGA:

Design was stable since a few weeks. Performed well in system tests with OptoTester.
Found one (non-standard) operation mode whereby tracker header information is misleading. This was fixed..
But at end of last week noticed a formatting error. Very hard to find except by automatic checking program. Problem wasn't there 2 weeks ago. We do have a version that corrects effect, but some more work is needed to understand why.

VME FPGA:

Saeed has taken over design from Ed.
Latest design working well in system tests.
Only minor change now to do is slowing down Cflash loading clock. Suspicion occasional failures of FPGA nr 7 (and 8?) to load could be due to driving JTAG chain over spec. Or some source of noise on our JTAG cables?
One minor change still desirable related to resetting of external clock DCMs. This would avoid hardware resetting of board when TTC clock is removed.
Decided not to do automatic reset after clock change (this can be done by software.)

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Get 2nd VME64x test crate operational	Done, on loan to CALICE	IC	
Get TTCrx clock output working.	Done	ST/JC	
Get TTCrx L1A output working.	Done	ST/JC	
Measure and adjust fine clock skews.	Done	EF	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Complete analogue mods and ship 005 to CERN	ST/JC	31-10-03
Finalise and test BE and VME Firmware release for CERN	ST/JC	31-10-03
Hand over of Firmware designs of VME and Delay FPGAs	EF/ST	31-10-03

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 38**		
Project Manager: J. Coughlan **Date:** Monday 27-October-2003		**Sheet: 2** **of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.5**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
17	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
18	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
20	New version OptoRx at RAL	01.04.03		21.07.03
21	FEDv1 Interim Review	08.09.03		11.09.03
22	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
23	Ship 1st FEDv1 to CERN.	30.09.03	31.10.03	
24	Ship 2nd FEDv1 to CERN.	28.11.03	28.11.03	