Project Monitor Form

Project: CMS FED **Date:** Friday 27 May-2005	**PMF number: 55** **Sheet:** 1 **of** 2

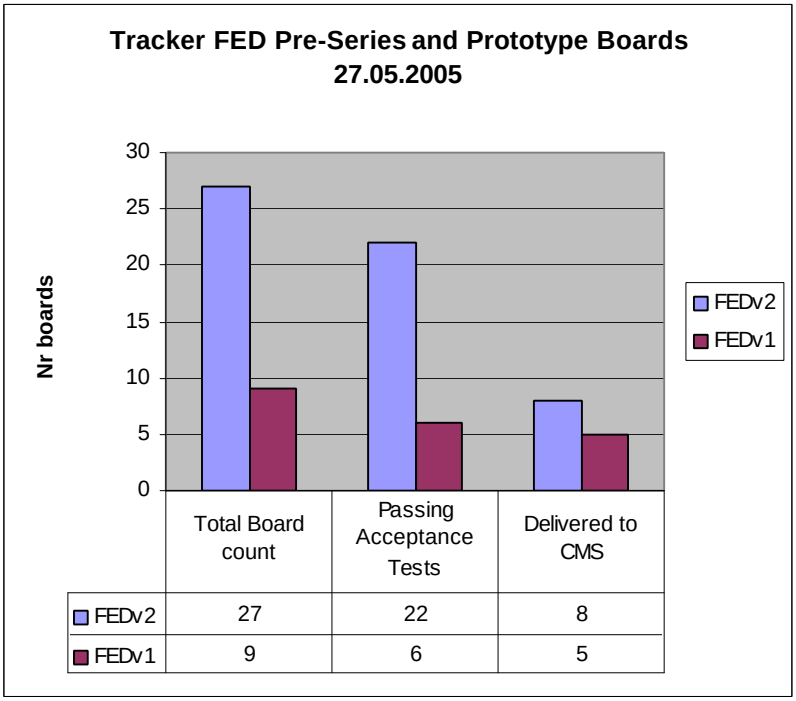
Project Implementation phase.

FEDv2

Manufacture of Pre-series
Production of 5 + 20 off FEDv2:

Summary of board status on web.
5 boards still to complete tests.

5 more pre-series boards shipped to CERN today (ser nrs 33-37).
Loaded with ACE 06_05_05 ; VME 21_03_1D



Meeting was held at eXception Calne on May 25th to review the Pre-Series and plan the final Production.

Reviewed the detailed list of faults found on last 20 boards.
-LED shorts (due to incorrect part size will be correct on production)
-Resistor net shorts/opens (part is difficult to assemble, eXception to test with varying solder masks)
Other minor faults

Production plans
ORx to be machine assembled. Samples obtained from CERN for re-profile of ovens.

Circuit schematics and layout unchanged from v2. Minor component values changed.
Increase DC converter hole size for conventional assembly. Update drilling drawing.
RAL to send updated Design Files, Ordering List.
Go to revision PC3205M/3

We will try for the first available assembly slot in July for first production batch of 50 boards. The first couple of boards would be tested at RAL within a 48 hour window (weekend) before giving go ahead for remaining top-side assembly.

Full Crate Tests

The spare LHC crate was eventually received at RAL on 21.04. This crate and the existing FED Tester crate are now installed in the CERN rack. The extender box to interface to the SLINK PC is also working.

Optical splitter board was obtained from Jan and is now installed and working in FED crate. Ivan has made a front panel to support it and will have some more manufactured. More fibres are on order to drive all16 FEDs.

Before Greg left he was able to successfully release the new adapter card to interface the FED Testers to the TTC system. James' new Multi-FED test software is now running at RAL for full crate tests.

Results:
Testing with full crate of 16 FEDs. Nothing unexpected seen.
Total power and current ok.
Readout from several boards over VME ok.
Power up ok after mod to resistor on OTemp line (below).
Programming of 16 boot VME EPROMs on chain via J0 backplane card is working.
Temperatures as expected, without water cooling (some boards are powered down if running crate for long periods).
Representative from company providing chiller for water cooling is visiting today.

Design Testing :

The earlier powering and reset problems observed on some boards has been cured by changing a resistor value on the Over Temp shutdown signal. This change will be carried out on all pre-series boards and for production.

One of the new FED Kits was loaned from CERN. Using this kit the S-LINK Zero-Suppressed readout on FEDv2 boards are now working without CRC errors under all readout conditions up to 400 M triggers per occupancy setting.

Request from Karl Gill to measure board to board variation in clock propagation delay through TTCrx chips.

Transition Cards :

Final version of Transition card (clock compatible with FEDv2+ only) has also been tested successfully at RAL with pre-series boards.
The length of the final DAQ SLINK CMC Transmitter card has changed slightly from FED Kit version, but still fits on Transition card ok.
A new Front Panel has been designed for final Transition card.

It has been agreed that RAL shall take over responsibility for the procurement of production quantities of the Transition cards. The design files are being handed over to Saeed who will manage this production. Project change order will be required.

Firmware :

BE / VME FPGA:
Tested checking of BX synchronisation.
Matt Pearson implemented the low level methods to access the features introduced into the design over the last few months. But he was unable to test them before he left.
Added some more Front Panel LED signals.
Added FED ID register = $00000fed at fixed location for identifying boards.
Resync command response needs minor updating (remove 21 micro-sec wait) to match new requirements as requested at Resync meeting at CERN 11.05.

FE FPGA:
Osman has implemented a Fake Frame generator.
Initial tests show that the basic functions are working, but there are some timing adjustments still to be done to obtain to get valid outputs on the first data sample.
Temp sensor I2C readout stopped working in latest VHDL version with Fake Frames.

Assembly Plant Testing

An area on the assembly floor has been set up at for FED testing.
Equipment: Boundary Scan kit is at RAL. PCs are on order.
2 x production 9U crates are expected to be available at CERN by June 8th Arrangements are being made to have these shipped to UK asap. Then need to swap these with existing crates at RAL. This is the critical path item.
Need one more SBS VME bridge (second one at Imperial?)

Contracts:
Good progress has been made recently.

The draft agreement from CERN was received last week. The payment and execution schedules have been updated and some minor amendments have been made by Tony Wells.
A project code is being set up in EID devoted to holding the funds from CERN to cover the payments for the eXception contract.

The final costings for 500 boards have been agreed with eXception with handling charges for the free issue components, including ORx modules.
The production contract document was released to them this week.
An order was placed in advance to purchase long lead items.

Forward Look

Activities, objectives and resources for the next 6 months …

- Production and acceptance tests in UK.
- How do we exploit/contribute to B904 integration centre?
- Remaining Firmware requirements and associated low level software.
- Higher level software tasks , calibration, run initialisation procedures …etc
- +++

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
List kit needed for full crate tests	Done. Obtained from CERN.	JC	
Order chiller unit	Company rep at RAL this week	IC	31-01-05
Stock check and spreadsheet of remaining FED components	Partially done. Unused kit returned.	IC	11-02-05
List kit needed for full crate tests	Done. Requested from CERN.	JC	
Install crates in rack	Done.	IC	
Complete route cards for preseries	In progress	IC	29.04.05
Release first draft of final contract to Geoff	Done	JC	
Order long lead components	Done	JC	
Implement SLINK new output clock firmware	Not required. SLINK now working at 80 MHz	ST	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Order chiller unit	IC	29-04-05
Stock check and spreadsheet of remaining FED components	IC	29-04-05
Complete route cards for pre-series	IC	29-04-05
Arrange for signing contract with eXception	JC	10-06-05
Obtain quotes for Transition card production	ST	10-06-05
Obtain 2 9U crates for Assembly tests	JC	17-06-05
Obtain PCs for Assembly tests	IC	17-06-05
Fix remaining pre-series boards	IC	30-06-05
Ship 10 more pre-series boards to CERN	IC	30-06-05

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 55**		
Project Manager: J. Coughlan **Date:** Friday 27 May-2005		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05	17.06.05	
31	FEDv3 tape-out	06.04.05	03.06.05	
32	First FEDv3 boards at RAL	13.07.05		
33	Production of 500 FEDv3 starts	08.09.05		
34	First FEDv3 at B904 Prevessin	30.11.05		
35	First FED installed at USC55	17.11.05		
36	Last FED installed at USC55	26.07.06		
37	Power on Tracker	01.08.06		
38	Readout test with Tracker	01.10.06		
39	LHC test run	02.04.07		