Project Monitor Form

Project: CMS FED	**PMF number: 13**
Date: Wednesday 27-March-2002	**Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

Rob had discussions with Xilinx rep re Non Disclosure Agreement. This should give us longer term pricing estimates. It may also be possible to obtain some IP for VME interface and JAM player.

Manufacture:

Improved quotes from Impact Memec for 2M and 40K parts. Delivery on 6-8 weeks lead time. Ordered 20x 2M and 60x 40K.

AD9218 and AD8138 parts have arrived sufficient for 10 FEDs (but see analogue discussion below.)

Quotes requested on power switchers.

Front End Module:

James verified in simulation and on test board that 2 stage opamp (using 8138, with resistorless gain of 2, followed by 8131) solution satisfies circuit requirements and does not suffer from problems of single stage solution. He has investigated DACs to drive Voltage offsets and has identified a number of suitable parts (nb 12 channel parts wouldn't be available until June.)

Meeting held with Mark Raymond from Imperial College and Marcus to review analogue circuit requirements based on latest OptoRx specs. Basic single stage (8131 or 8138) and two stage options (8138 + 8131) presented. It was agreed that 2 stage option was only one technically acceptable. It was also decided to run Opamps on +/- 3.3 V rails to ameliorate increased power demands. James will verify whether this latter option is ok in practice on test board.

However following meeting Mark suggested an alternative Opamp Elantec EL2140C which appears be able to satisfy single stage option demands. James has requested samples to make equivalent tests to those done with 8131/1838 circuits. We will ask Chris to go ahead with a layout with this part.

A further telephone conversation with Francois clarified and confirmed a few remaining questions concerning OptoRx specs. Heat dissipation on production modules will be through the top of the module and leads (ie not bottom). It will be sufficient to have one per OptoRx for voltage offset (DAC also permits test feature desired by customer.) There is decoupling on chip and in module for power supply rejection (separate for VCC1 , VCC3.) A graph describing effects of OptoRx offset control settings has now been produced by Jan Troska.

Chris has concentrated on digital part of FE module and has entered FE FPGA part in library (by hand.) He is now waiting for signal layout on FPGAs.

Firmware:

Delay FPGA:

Ed will pass his list of signals to Chris.

Ed has also made a graph of clock skew versus DCM setting. The plot is monotonic and best estimate for skewed clock jitter is approx 300 ps (which is in line with expectations and acceptable.)

He is now updating the documentation before starting his placement with Marcus.

Board level:
Saeed updated power table based on 2 stage opamp solution assuming running on +-/ 3.3 V rails (cf +/- 5V.) Typical values just within spec but max consumption will exceed LHC crate specs. Saeed has identified suitable switchers to derive 1.5 V and –5 (or –3.3) V. Quotes requested. In this scenario we use 48V to derive –3.3 V supply and 5V to drive +1.5V.

Confirm 12 layer board with 4 power (incl 2 Gnd) + 8 signal planes, although it may still be possible to reduce to 10 layers (4 + 6).

Power estimation tools for VirtexII are now available. Estimates for delay chip redone. Important to redo estimate for FE FPGA.

It was agreed to adopt 3 chain JTAG solution for both test and FPGA configuration (with option for jumpering to one single chain.)
Configuration will be through either JTAG connector, VME FPGA + Flash or System ACE (single chain.)

Review of options for bus widths between FE FPGAs and BE FPGA and between VME FPGA and BE FPGA. Agreed to be safe and adopt wider parallel buses. Should not be a problem for tracking, but Saeed will discuss implications with Chris.

Quick review of remaining back end components done.
VME FPGA chosen: compatible VirtexII family (FG456 2V250, 2V500, 2V1000.)
Also parts for QDR SRAM, configuration EPROM, buffers identified. Quotes will be requested immediately after Easter.

Actions from the previous PMF

Action	Status	Who	Target date
Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	Done	EF	
Produce 1st order FE module analogue component layout.	Waiting for schematic with Elantec opamp.	CD/JS	25-02-02
Find out from Paul Hardy whether it is possible, and if so how, to automatically generate Xilinx FPGA symbols in CADENCE.	Done. Was not possible within permitted time, but FPGAs were put in by hand.	RH/CD	
Produce user manual for Delay chip.	New version in progress.	EF	30-04-02

Verify fit of final design on evaluation board.	Done. Not feasible on evalutaion board. But designs for both C and CES sythesised.	EF	
Order FPGAs for batch 0.	Done.	JC	
Finalise and document JTAG test and configuration chains	Scheme agreed. To be documented.	ST	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Produce user manual for Delay chip.	EF	30-04-02
Pass Elantec opamp analogue schematic circuit to Chris.	JS	08-04-02
Pass details of any remaining components eg DAC to Chris.	JS	08-04-02
Update FE module analogue layout with Elantec opamp.	CD	15-04-02
Repeat measurements a la AD devices with Elantec opamp circuit on test board.	JS	15-04-02
Repeat simulations a la AD devices with Elantec opamp model.	JS	15-04-02
Identify and obtain quotes on BE components: VME FPGA, QDRAM, EPROM.	JC	08-04-02
Revise power/current tables for Elantec opamp option.	ST	08-04-02
Revise power/current tables for FE FPGA in VirtexII model.	ST/WG	15-04-02
Send analogue circuit diagrams to Francois Vasey.	RH	08-04-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 13**		
Project Manager: R. Halsall **Date:** Thursday 27-March-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.0**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	**Project Spec sign off**	**21-12-01**		**05-02-02**
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	11-03-02	
5	FE Module Feasibility Review	28-02-02	11-03-02	
7	**Board Level Feasibility Review**	**04-03-02**	**08-04-02**	
8	Delay FPGA Interim Review	31-01-02	04-03-02	
9	Front End FPGA Interim Review	31-01-02	04-03-02	
10	Back End FPGA Interim Review	31-01-02	25-03-02	
11	VME FPGA Feasibility Review	28-02-02	25-03-02	
12	Clock FPGA Feasibility Review	28-02-02	25-03-02	
13	Release Test Plan Document	22-02-02	08-04-02	
14	FE Module Final Review	30-04-02		
15	BE Board Final Review	10-05-02		
16	Full Board Design Final Review	31-05-02		
17	**IDR Customer Production sign off**	**10-06-02**		
18	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**26-07-02**		
19	OptoRx for Batch 0 at RAL	26-08-02		
20	**Batch 0 Opto Assembled boards at RAL**	**01-11-02**		
21	Batch 0 review	06-01-03		
22	**Batch 1 (8 off) Assembled boards at RAL**	**21-03-03**		
23	**Delivery Batch 1 to CERN completed.**	**11-07-03**		