Project Monitor Form

Project: CMS FED **Date:** Friday 26 Nov-2004	**PMF number: 51** **Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs
Last 4 working spares shipped to CERN.

FEDv2

Extensive tests have been carried out on FEDv2 with new S-LINK Transition cards (see report from James Leaver).

Problems with 4 stuck S-LINK data lines (UD16-19 and only on FEDv2) eventually discovered to be due to change in the default pin configuration with new FPGA tools (ISE 6.x dual purpose SELECT MAP parallel configuration lines). Took a lot of investigations to understand this. Suspected Transition card, FEDv2 pcb, crates, firmware!

CRC errors due to changes in timing with LVDS S-LINK clock. Also some confusion due to unexpected insertion of CRC code by FEDKit PMC. Some CRC errors remaining at high occupancy under investigation. Not clear whether problem is in data transfer or CRC calculation.

Data from 2 mixed events were observed at high rates. Eventually traced to occasional mistake in QDR write pointer during S-LINK back pressure. Fixed.

Cross talk measurements show some effect of a pulse on the immediate neighbouring ADC channels (see report from James Leaver). Effects are probably tolerable.
Fibres with mistimed headers cause unacceptable interference and need to be avoided.

Noise measurements on FEDv2 consistent or slightly better than previous on FEDv1. No anomalous noise on 5th channels.

Testing results so far indicate that FEDv2 design could be used for production with only minor component value changes on FE analogue (see below)

Manufacture
Agreed schedule with DDi on 2nd Nov for Pre-series production of 25 off FEDv2:

Place order on 15th Nov to manufacture 25 PCBs using Final v2 design (c.f. quotation design used for 18 & 19). Additional information provided in drilling drawings to specify acceptable board thickness.

Assemble 5 off starting December 13th , **delivery 5 off 1st week in Jan 05**.
Then 2 weeks for test before assemble 20 off go ahead in Jan 24th , **delivery 20 off expected week of Feb 21st.**
Schedule is tight to commission individual boards and complete the full crate tests before start delivery to CERN for LSA.
During Tracker week various LSA centres put forward their electronic delivery requests. Overall

totals and schedule for FEDs is still unclear. Aiming for **delivery of first boards by end of May 05.**

Assembly will be on main Siemens production line.
Free issue components. Boundary Scan at RAL.

Production quantity components at RAL for QDRs and EL2140C (Opamps).
NB Bulk of production TTCrx/PIN components will go to DDi.
On final checking of kit we found a couple of missing components. However, these are expected to be in hand by next week when kit is due for collection (should also have new load resistors).

Design Testing :

Tests by Stefanos of FE Analogue component values using modified board nr 02 were postponed until after October test beam. Initial results indicate Load Resistor should be reduced to about 62 Ohm to maintain flexibility in link gain settings. Capacitor values to remain unchanged as no significant improvement to settling time observed. Tests need to be repeated on a FEDv2.

Firmware :

Temp sensor I2C errors fixed (in firmware).
System ACE interface for in-situ Compact Flash reprogramming is working again.

Implementation of List of Missing Features in URD in progress.
TTC chan B short and long commands e.g. Resync now being implemented.
Proposal for reduced header format and additional error monitoring registers presented at this meeting.

<u>Assembly Plant Testing</u>

Procedures have been optimised. Draft of document describing test plan to be carried out at Assembly plant released. DDi head of test section due to visit next week.

The backplane pcb, which is used to distribute the JTAG programming line along J0, has been tested successfully with 2 FEDv2s. A total of 5 pcbs have been made.

VME loop back card for Boundary Scan has been delivered and tested successfully (5 cards made).

Rack at CERN to be inspected by Ivan in December. Space in R25 lab identified.

Ivan is investigating extensions to JTAG Boundary scan products.

<u>Other Items</u>

CERN 25 nsec beam test took place in October using same 4 FEDs as in May.
FEDs with latest standard release.

ACE File: 16_07_04_1500 = (Delay 02_1B ; FE 03_16 ; BE 02_43)
EPROM : VME_03_0F

NB Still need to upgrade old boards at CERN (to be FEDv2 compatible) by simple addition of couple of LVDS clock resistors.

Moved PCI-X PC from PPD to R25 lab (now named cmsfed1.te.rl.ac.uk). Only one of our SBS cards is compatible with PCI-X.

Tender :

Tenders from 7 companies received on 27th October.
Adjudication panel met on 8th Nov.
3 companies selected for Framework contract DDi, STI , Cemgraft.
Meeting held with DDi on 18th Nov to discuss details of contract, testing etc.
Awaiting estimate of testing costs following visit to RAL.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Verify design of FEDv2 before pre-series.		IC/JC	Done
Testing Specification document for Assembly company	Draft released	IC	Done
Implement Firmware for TTC chan B commands	Registers implemented	ST	06-12-04

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Implement Firmware for TTC chan B commands	ST	06-12-04
Implement reduced Tracker header format.	ST	07-02-05
Implement error monitoring spy channel.	ST	07-02-05

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 51**		
Project Manager: J. Coughlan **Date:** Friday 26 Nov-2004		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Award Tender contract	09.02.05		
31	FEDv3 tape-out	06.04.05		
32	First FEDv3 boards at RAL	13.07.05		
33	Production of 500 FEDv3 starts	08.09.05		
34	First FEDv3 at B904 Prevessin	30.11.05		
35	First FED installed at USC55	17.11.05		
36	Last FED installed at USC55	26.07.06		
37	Power on Tracker	01.08.06		
38	Readout test with Tracker	01.10.06		
39	LHC test run	02.04.07		