Project Monitor Form

Project: CMS FED	**PMF number: 33**
Date: Thursday 26-June-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Front-panels and other bits arrived on 23.06
Should start shipping batches next week.
CMS are happy if they arrive by Tracker week.

We have also had the “spare” 10 boards assembled (but of course untested.)

FEDv1:

Manufacture

Additional delay caused by uneven edges and “pips” on boards leading to misalignments on assembly machines.
2 boards (one with 8xOptoRx) now expected at RAL tomorrow Friday 27th June.

Plus 1 board was returned yesterday by Assembly company partially done (noticed a “scar” seen over 6 tracks.) PCB manufacturer was contacted and sent tech manager. Fixed with scalpel. Looks like "dirt” got trapped between 2 layers (silkscreen or resist?). Claimed this would not have caused shorts as auto tests would have reported such a problem. Will check history files. We’ll use this board for power tests.

Firmware

Delay-FPGA:
Some time spent investigating problems with clock skewing (was not covering full 360 degrees.) Problem eventually localised to serial command decoder and now fixed. Simulation had worked perfectly? It wasn’t possible to use ChipScope easily in this design hence harder to debug, back to using a couple of test pins and a real scope!

FE-FPGA:
Now observing “almost realistic” APV tick and frames in Scope mode. Data is generated in BE test design and fed by cable to Electrical test card inputs. We can also adjust data level within frame w.r.t. to header level.
Just started to set-up FE into Frame Finding mode. See “lock” signal come on and off, but as yet do not observe the Frame Sync signal (indicating valid headers are found.)

BE FPGA:
Now testing with final design on FED. Started by debugging serial command interface by optimising clock distribution (same procedures as in test design.). Lots of detailed debugging of address and data patterns using ChipScope. Nb We can’t do trick of locking this design in place. But ChipScope results seem reliable so far, albeit we can’t risk observing too many lines at once. Addresses and FE data entering QDR now seem in correct order. But precise timing/alignment

can only be checked by reading out memories. Now trying to get readout of QDR to work.

VME FPGA:
Implementation of VME-Link receiver is in progress. Should have something to test early next week.

Other Firmware
A possible work around (tying down design with Relational Macros before adding ChipScope) to permit reliable use of Chip-Scope in our designs seems to work on FE design, but not on BE design?

Rob has adapted Xilinx reference design (to match our S-LINK requirements) for "Channel Link" tests on development board.
He has observed counter data being transferred over 2 metres on his special cable (5 lines?) at 24 MHz (7:1 Mux => 168 MHz clock on cable.)
No checks on bit errors yet. Can go higher on clock speed.

Other Activities
Existing problem reports are being collated and brought up to date for purposes of CALICE project review. CALICE are using the rear-end of FED board design.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Start Test FE to BE FPGA and QDR data write path.	Done	ST/JC	
Start Loop back test on FED with apv headers from BE.	Done	IC/JC	
Start test on FED of VME-Link receiver.		EF/JC	04-04-03
Send first batch of FED-PMCs to CERN.		JG/JC	09-05-03

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Send first batch of FED-PMCs to CERN.	JC	04-07-03
Start test on FED of VME-Link receiver.	EF	30-06-03
Observe Frame Finding data capture.	IC/JC	04-07-03
Observe correct QDR data readout.	ST/JC	04-07-03
JTAG new boards.	IC	04-07-03

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** J. Coughlan **Date:** Thursday 26-June-2003		**PMF number: 33** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off &PCB Tape Out**	**07.10.02**		**06.12.02**
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**		**22.01.03**
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		