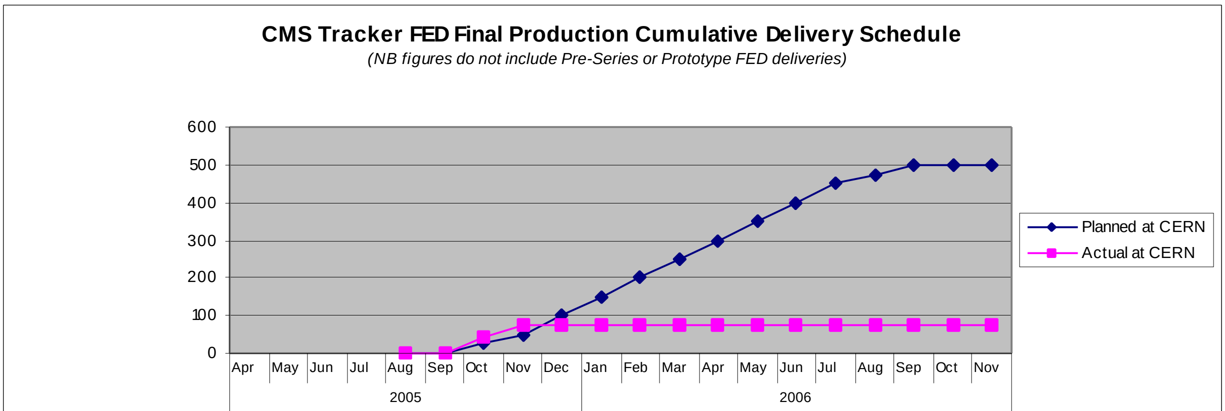
Project Monitor Form

Project: CMS FED **Date:** Fri 25 Nov-2005	**PMF number: 58** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

Board Deliveries: Remains on schedule.
2nd batch at CERN bringing total to 75 boards.
3rd batch of 35 ready to ship today. Delivery will be by air freight to Geneva with instructions to pack in crates. Previous delivery was delayed in Paris by courier misunderstandings.



	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov
	2005									2006										
Planned at CERN					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
Actual at CERN					0	0	40	75	75	75	75	75	75	75	75	75	75	75	75	75

Production:
Assembly plant test setups working well.
A couple of visits to sort out some Boundary Scan system issues.
Helping out with a few boards that were giving problems.
Collected first lot of detailed Test Results information (passed to James).

Xilinx System ACE chips are back in production. It was not necessary to use parts from alternative sources. These will be kept as spares.

A further 1,175 ORx were sent from Imperial to eXception this week.

Final quantities of TTC fibres and couplers now at RAL (UK supplier).

Testing at RAL:

Just keeping pace with board deliveries from eXception.
Boards from 4th assembly batch are now arriving at RAL.

Board quality arriving at RAL remains good. Minor issues in finishing (e.g. DC-DC lead trimming) now resolved. One with damaged connector returned.

Full details are in Production spreadsheet.

During 2nd batch burn in tests we noticed that a couple of boards in fully populated crates were not

starting up. Intermittent problem. And more of an irritation. Power on boards was checked and ok. But VME FPGA was not programming until reset switch applied.
Eventually understood as only happening with backplane J0 pcb in place. This is used to program chain of EPROMs in-situ. So problem is not on FED. Likely some noise pickup on pcb. A fix to pcb already found, will replace pcb at 904 next visit.
Plan to flash LED on Front Panel to indicate FPGAs are running.

Also found couple of boards with problems traced to flux residue on VME connectors. In future will clean at RAL.

The “final” LHC Power supply blew during full crate tests. Returned to CERN and replacement obtained. CERN inform us failure has happened on 5% of these PS.

A couple of boards exhibit a strange word swapping behaviour in the data readout. Still under investigation. This causes Assembly Test to abort.

CERN

Tracker Week:

Inspected rack mock up of Optical cabling scheme in Jan’s lab. Arrangement looks very good.
Expect to install FEDs before cabling is done.
The cable support trays used during installation must be such that air flow to FEDs is not obstructed to permit racks to be powered for DAQ tests.

Electronics Integration Meeting:

DAQ Production of FRL (SLINK receivers) and CMC transmitters completed. Testing will be completed by January.
Aim to test FED + Transition + CMC as unit. And full crate of FEDs as unit for installation.

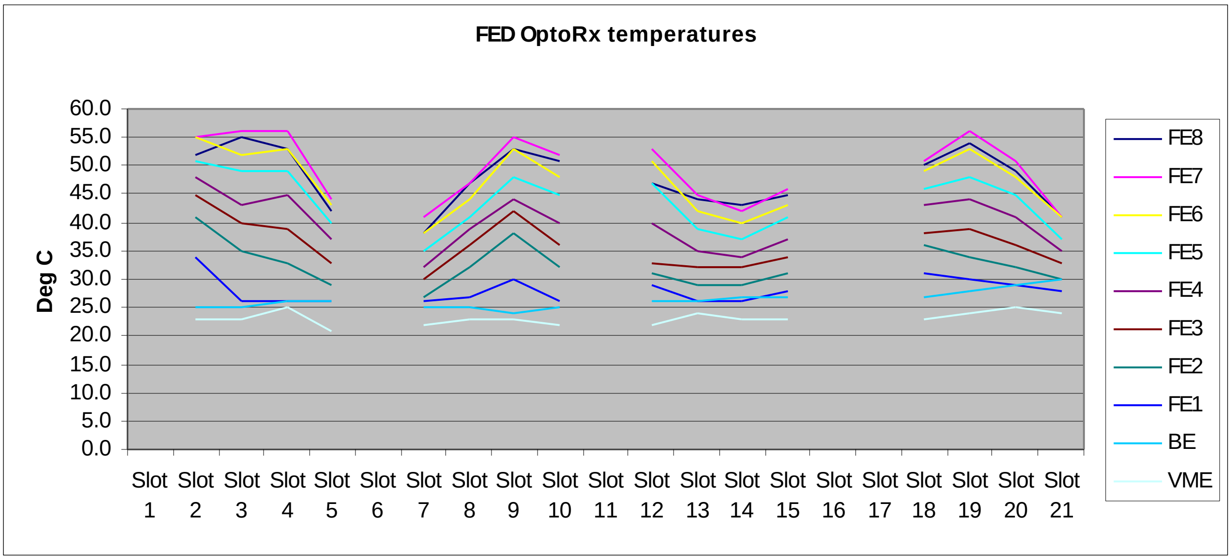
DAQ to add another event CRC check in CMC firmware.
DAQ have implemented SLINK down signal on CMC.

FMM (throttle cards) also made and under test. But DAQ group tests show there are unexpected problems with noise on FMM links. They have changed to shielded cables and now recommend grounding at both ends.
Tests with our Transition cards are urgently needed before we complete production.

DAQ will provide autonomous SLINK cable testers for installation.

B904 :

Full crate tests at 904 were delayed due to a problem with the cooling system. After a lot of valiant effort this was finally solved by cleaning the filter at the input valve in the 904 lab. Temperature measurements are consistent with those obtained at RAL (RAL results below).



NB The ADCs should be disabled outside data acquisition runs. This reduces max temperatures by further ~ 5 degrees.
Adding blanking cards in empty slots may also help.

Tests with 3 FED crates in one rack now in progress.

Firmware (see also Oz slides) :

The VME BLT read has been increased a further few percent.
Note that measured rates depend on how many FEDs are in the crate and VME bridge type and positioning variation few percent.
Verified with expert that CAEN VME bridge does support BLT64 , but not tried.

Mechanism for SPY channel capture of Frames agreed. FE FPGA part implemented. Delay FPGA to do.

Pedestal loading in FE VHDL version debugged. Auto Increment of addressing for Read and Write now working.

Odd behaviour in ZS Fake Frame cluster finding in FE VHDL is now fixed (Fake DCMs removed).

Q. When can we adopt VHDL as standard FE FPGA release? Needed for Fake Frames.

TTC channel B commands reviewed again.

Request for “L1 Trigger” on TTC channel B pending decision on test kit requirements.

Integration Tests:

Slawek Tkaczyk has taken charge of coordinating Tracker Electronics Integration.

First SLINK FRL readout with one FED + Transition card/CMC and final cable (length?) carried out successfully at Cessy Pt5. Using internal clock/triggers.
2 FED merging to FRL test next.

FMM card throttle test needed before remaining 400 Transition Card production.

Software:

Software to handle newer Firmware registers being implemented.
See slide from Jo.

Other Items:

Final 6 Pre-Series boards sent to CERN 17.10.05. Needed for LSA test centers.

Some TTCoc Front panels sent to Jan. Blank Front panels sent for 904.

Discussed Laser Alignment group requirements again at CERN. These are already satisfied by FED.

New PPD Director John Womersley has visited the FED Testing lab.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Fix remaining pre-series boards and send to CERN.	Done	IC	
Test ZS lite firmware.	Simple test done.	JC	
Test 10 bit to 8 bit FE firmware.	Not attempted	JC	28-10-05
Update Transition Card BOM.	Awaiting FMM test	ST	28-10-05
Have first batch of production FEDs ready for delivery to CERN.	Done.	IC	
Implement Firmware for automatic TCRIT shutdown.	Done.	ST	
Order TTC fibres and couplers.	Done.	IC	
Attend CERN Safety Training	JC still to do	JC	28-10-05
Optimise FED slot arrangement in cooled rack.	Done at RAL	IC	
Summarise FED Finances.	Done	JC	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Test 10 bit to 8 bit FE firmware.	JC	28-10-05
Update Transition Card BOM.	ST	01-03-06
Test DCM firmware from GCT group	JC	27-01-06
Contact Attila to arrange FMM tests	JC	20-01-06
Carry out end of year review at eXception	JC	23-12-05

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** J. Coughlan **Date:** Fri 25 Nov-2005		**PMF number: 58** **Sheet: 2 of 2**		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05	22.07.05	28.07.05
33	Production of 500 FEDv3 starts	08.09.05	27.07.05	01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05	30.10.05	27.10.05
35	First FED installed at USC55	17.11.05	01.05.06	
36	Last FED installed at USC55	26.07.06	31.09.06	
37	Power on Tracker	01.08.06	30.11.06	
38	Readout test with Tracker	01.10.06	01.02.06	
39	LHC test run	02.04.07	01.07.06	