Project Monitor Form

Project: CMS FED **Date:** Thursday 25 September-2003	**PMF number: 37** **Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Verified that Jonathan is not expected back from TA service until the end of the year.
It was planned that Ivan would start testing PMC cards in a couple of weeks. Test bench needs some setting up.
However on 24th September Jan Troska reported problem with incorrect parts on one of latest batch of PMCs. Now under urgent investigation.

FEDv1:

Manufacture

6 FEDv1 now in assembly are expected back next week.

Ser 003 (without OptoRxs) prepared for loan to CALICE.
7th FE FPGA on 003 sometimes refuses to load from Cflash. Always can reload via JTAG chain?
This effect has now been observed on 2 boards, but it is not persistent.
Has it ever been seen at Imperial?

Second small 9U crate (intended for power tests) to be loaned to CALICE if LHC crates are delayed.

3 LHC crates (with 6U kits to assemble) should be on their way to RAL.

Interview arranged on Oct 6th with Procurement Officer rep for INS, Lindsay Glover.

Analogue

Matt's measurements on evaluation board (with standard FED AD9218) show same pre-pulse undershoot as observed on FED.
Rob has suggested trying ADCs from another batch for comparison.

OptoTester with FED system tests
Remotely operated Scope and Frame Finding tests at Imperial feeding frames from FED Opto-Tester show some signs of working, but several effects yet to be understood. Firmware at IC needs updating (but wouldn't explain these effects.) Opto-Tester program has been set up nicely for these debugging tests.

We now need to concentrate our effort in one place for a period to understand details of FED operation with external inputs. This really needs to be at RAL where the firmware can be debugged and modified.
Proposal that Greg brings the FED tester to RAL starting in the week of 6th October and spends some time with us.
This also requires that Matthew and Gareth have got the latest software Jonathan is now using at

Imperial up and running at RAL to allow us to get access to the full data readout.

TTCrx

In tests at Imperial, with assistance of Greg ,after last meeting first with TTCvi(mk I) & TTCvx and then with second TTCvi(mk II) & TTCex we observed TTCrx ready signal on when fibre was connected and saw good clock on TTCrx output pins.
Using the IC TTCvi(mk II) & TTCex at RAL we also saw clocks on TTCrx output and was able to switch to TTC 40 MHz clock on FED.
(NB We could still not generate clock using original pair of TTCvi(MkII) and TTCex card given to RAL (suspect TTCex?)
We still have some problems however.
1. We cannot generate sensible L1A triggers through to TTCrx. Suspect problem is in signals from TTCvi. No signals on chanA are seen when random triggers are enabled?. Although all other indicators say triggers are being generated. In principle there should be very little to set up on TTCvi.
2. TTCrx still powers up often in a state in which it cannot be addressed or reset.
3. TTC ready signal still occasionally indicates missing encoded data.

The only system to compare at RAL is in PPD ATLAS. They use TTCvi(Mk1) and TTCvx like at Imperial. Have looked at signals on these cards with their expert and it works as I would expect.
Status : Still under investigation.

Firmware

Delay-FPGA:

Whilst doing final tuning of skew settings we discovered that fine skews were no longer operational. One reason was caused by inadvertently setting an illegal reset value. Second change was necessary because clock distribution from FE had changed in the last couple of months. Also had to set back some options that were used when running with engineering samples, but we know these are not ES!
Skewing is however working and is now being fine tuned. But there is still one odd effect to iron out in serial command interface causing every second command to be ignored.
Ed will remain on project until these are corrected.

FE-FPGA:

Problem with empty 2nd data channel of each FE FPGA traced to bit of test code introduced whilst testing DDR transfers in firmware and fixed.
TrimDAC is now reset by Firmware when a VME reset is sent. This should cure odd data observed on 12th channel of each FE FPGA.
Bug fixed in ADC control settings register. Can now read and write properly.
Updated release **FE_02_04** (FE_03_04 for 1500)

Design is being handed over to Saeed for implementation of full serial interfaces to LM82 and TrimDACs.

BE FPGA:

Proper I2C interface to LM82 Temp sensor implemented in firmware. Now reading out chip temperatures. This block is to be ported to FE FPGAs.

Minor changes introduced to rationalise trigger logic.
Control register default settings made more sensible.

Switched to using Delay Skew 1 clock from TTCrx (supposed to be guaranteed on at power on). Now passed to VME as single ended (as LVDS resistor was missing).

Added dedicated software TTCrx reset to avoid hang ups whenTTC clock is selected.

Some preliminary discussions concerning firmware needed for Laser alignment triggers.
Best option would be by using main data stream and swapping between cluster mode and raw data mode if there is sufficient time in “calibration” orbits.
Mostly affects BE design.

VME FPGA:
A status register to indicate completion of serial commands has been added.

Successful clock change should now cause a general reset to be issued to the board.