Project Monitor Form

Project: CMS FED **Date:** Friday 25 Feb-2005	**PMF number: 53** **Sheet:** 1 **of** 2

Project Implementation phase.

FEDv2

Manufacture of Pre-series
Production of **5 + 20** off FEDv2:

Assembly of first 5 boards completed fairly smoothly. Some improvements to the conventional assembly were suggested. Boards arrived during week of 24th Jan.
Quality of Assembly was very good.
Bds 21 (now at Imperial),23,24 passed both Bscan and LabView tests 100% first time.
Bd 22 passes Bscan but has 4 bad channels. Eventually traced to a damaged FPGA. Soon to be reworked.
Bd 20 after minor repair now passes tests, but had some intermittent power resetting problems (which may have caused some spurious Bscan errors).
NB Analogue testing passed 100% on all boards.

A week was made up in testing permitting the next 20 to keep to original schedule.
Remaining 20 boards went through machine assembly are now in conventional assembly and Quality control.
We expect the first of these boards early next week and the remainder by mid March.

<u>FED deliveries and repairs</u>

2 FEDv2 boards nrs 18 (with 62 Ohm) and 24 were dispatched to CERN on 24th Feb.
ACE File: 22_02_05 ; **EPROM : VME_03_1b**
Either of these boards can be used by Stephanos.

FEDv1 nrs 05 and 13 arrived from CERN during tracker week .
Bd 05 had ancient firmware (too old to be compatible with my test software). Bd was upgraded to FEDv2 firmware and standalone readout tests pass ok.
Bd 13 did exhibit some odd intermittent VME readout errors (dependent on event size). Bd was also upgraded to FEDv2, which cured the problem.
Fast VME readout tests with FED Testers require us to go back to old style throttle cabling to the FED Testers. This must be done before returning these cards.
NB FEDv1 boards will only support VME event readout.

Design Testing :

Extensive tests of S-LINK and VME Zero-Suppressed readout using latest firmware on FEDv2 boards with high rate triggers has found no readout errors.

Occasional problems were observed on some FED channels during the automatic timing calibration (using APV ticks). This took some while to understand. James has developed some nice tools to diagnose. Fixed in Delay DCM firmware (see below).

Francois has agreed to sign off FED design once measurements have been confirmed on FEDv2 by Stefanos Dris.

Firmware :

Decoding of TTC chan B commands for L1A, BX ctr reset, Resync and APVE broadcast are tested and operational (as per Matt Pearson's TTC note). Handling of Calibration events during normal running is now being implemented.
A list of low level software needed to exploit these features is being drawn up.
The new Full Debug Tracker header format has been extensively tested and is now standard in V2 firmware. The new APV debug monitoring channel is also working.

The Delay FPGA design has been slightly modified (number of internal DCM steps reduced from 9 to 8) to cure problems observed during automatic timing calibrations. The table relating nsec offset vs skew setting needs to be re-measured and updated, although the change is expected to be small.

The BE FPGA technical description has been updated with full details at
http://www.te.rl.ac.uk/esdg/cms-fed/firmware/Documents/BE_FPGA_Technical_Description.doc
*The full debug information is also provided in VME registers for monitoring (needs testing).

Assembly Plant Testing

Further refinements to the testing plan and LabView application have been made. Testing references have been adapted for Rload=62 Ohm.

A test engineer from eXception EMS will spend a day or two at RAL during the testing of the next batch of 20 boards to gain experience of the procedures.

Final Acceptance Testing

It is proposed that the full crate acceptance tests be concentrated at RAL.
The rack from CERN has been moved (with a little effort) to our lab. Crates have yet to be installed. Solutions for cooling are still being arranged, although cooling is not necessary to start testing.
Missing Equipment. During tracker week Patrice Siegrist told us that we could have the last remaining LHC crate, but it required some repair. Also loan of an adapter for our SBS PCI card was possible. No news of progress on delivery since.
As last resort we may use our test crate temporarily, although it would involve considerable disruption and there is some risk of damage to boards owing to its poor mechanics
Greg is preparing hardware to interface the FED Testers to the TTC system, which will allow multiple FEDs to be triggered.
James is extending the Universal FED tests to permit flexible, multiple FED testing.

Other Items

Numbering Scheme
It is proposed to adopt today a FED channel numbering scheme suggested by Francois.

This has the advantage being unambiguous and still following the optical cabling order.

```
FE Unit/Ribbon   Fibre   OptoRx pin    DAQ Chan (S/W)
    8             12       F12           812          TOP
    8             11       F11           811
    8             10       F10           810

....
....

    1             3        F3            103
    1             2        F2            102
    1             1        F1            101          BOTTOM
```

Final Production:

The DDi Europe group underwent a management buy out effective 9th Feb. The management and technical staff have not changed. The new company agrees to take over all liabilities, contracts etc from DDi. RAL Finance is treating this as a simple change of name.
There has been no disruption of our pre-series production.
(The new group has severed connection with the DDi operations in the USA).
DDi Technologies (Assembly) Calne becomes eXception EMS Ltd
DDi Tewkesbury (PCB) becomes eXception PCB Ltd

Papers have been submitted for CERN Finance Committee in March.
A follow up meeting with eXception EMS to discuss contract issues is now proposed for soon after the CERN Finance committee decision. Meeting to be held at RAL.

INS procurement office is closing and the storage room will be lost shortly. We would like to move the parts we have in hand for final production to Imperial for safe storage with the OptoRx modules. Other items in FED stock will be moved into storage in our lab.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Implement Firmware for TTC chan B commands	Calibration event handling remaining	ST	06-12-04
Commission first 5 boards using LabView App	Done	IC	
Test first 5 boards using SLINK & VME readout	Done	ST/JC	
Mod nr 17 and 19 and send to CERN	17 and 19 modified.	IC	
Test new Tracker header format contents	Full Debug Done	JC	
Test new monitoring spy channel	Done	JC	
List kit needed for full crate tests	Requested from CERN.	JC	
Coordinate pre-series production with DDi	Done	JC	
Order chiller unit	In progress	IC	31-01-05
List kit needed for full crate tests	Requested from CERN.	JC	
Stock check and spreadsheet of remaining FED components	In progress	IC	11-02-05
Update Finance Ctte submission doc	Done	JC	
List kit needed for full crate tests	Done. Requested from CERN.	JC	
Implement comments and release new BE FPGA technical doc	Done.	ST	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Order chiller unit	IC	04-04-05
Stock check and spreadsheet of remaining FED components	IC	04-04-05
Install crates in rack	IC	01-04-05
Complete route cards up to FED nr 24	IC	04-03-05
List of equipment needed for JTAG	IC	11-03-05
Complete BE FPGA related missing features from Ian Tomalin's list.	JC	04-04-05
Document FED channel numbering scheme	JC	07-03-04

Release list of software needed for FEDv2 firmware	JC	07-03-04
Arrange for eXception test engineer to visit RAL	JC	04-04-05
Arrange for contracts meeting at RAL with eXception	JC	04-04-05

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 53**		
Project Manager: J. Coughlan **Date:** Friday 25 Feb-2005		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Award Tender contract	09.02.05		
31	FEDv3 tape-out	06.04.05		
32	First FEDv3 boards at RAL	13.07.05		
33	Production of 500 FEDv3 starts	08.09.05		
34	First FEDv3 at B904 Prevessin	30.11.05		
35	First FED installed at USC55	17.11.05		
36	Last FED installed at USC55	26.07.06		
37	Power on Tracker	01.08.06		
38	Readout test with Tracker	01.10.06		
39	LHC test run	02.04.07		