Project Monitor Form

Project: CMS FED	**PMF number: 53**
Date: Friday 25 Feb-2005	**Sheet:** 1 **of** 2

Project Implementation phase.

FEDv2

Manufacture of Pre-series
Production of **5 + 20** off FEDv2:

Assembly of first 5 boards completed fairly smoothly. Some improvements to the conventional assembly were suggested. Boards arrived during week of 24th Jan.
Quality of Assembly was very good.
Bds 21 (now at Imperial),23,24 passed both Bscan and LabView tests 100% first time.
Bd 22 passes Bscan but has 4 bad channels. Eventually traced to a damaged FPGA. Soon to be reworked.
Bd 20 after minor repair now passes tests, but had some intermittent power resetting problems (which may have caused some spurious Bscan errors).
NB Analogue testing passed 100% on all boards.

A week was made up in testing permitting the next 20 to keep to original schedule.
Remaining 20 boards went through machine assembly are now in conventional assembly and Quality control.
We expect the first of these boards early next week and the remainder by mid March.

<u>FED deliveries and repairs</u>

2 FEDv2 boards nrs 18 (with 62 Ohm) and 24 were dispatched to CERN on 24th Feb.
ACE File: 22_02_05 ; **EPROM : VME_03_1b**
Either of these boards can be used by Stephanos.

FEDv1 nrs 05 and 13 arrived from CERN during tracker week .
Bd 05 had ancient firmware (too old to be compatible with my test software). Bd was upgraded to FEDv2 firmware and standalone readout tests pass ok.
Bd 13 did exhibit some odd intermittent VME readout errors (dependent on event size). Bd was also upgraded to FEDv2, which cured the problem.
Fast VME readout tests with FED Testers require us to go back to old style throttle cabling to the FED Testers. This must be done before returning these cards.
NB FEDv1 boards will only support VME event readout.

Design Testing :

Extensive tests of S-LINK and VME Zero-Suppressed readout using latest firmware on FEDv2 boards with high rate triggers has found no readout errors.

Occasional problems were observed on some FED channels during the automatic timing calibration (using APV ticks). This took some while to understand. James has developed some nice tools to diagnose. Fixed in Delay DCM firmware (see below).

Francois has agreed to sign off FED design once measurements have been confirmed on FEDv2 by Stefanos Dris.

Firmware :

Decoding of TTC chan B commands for L1A, BX ctr reset, Resync and APVE broadcast are tested and operational (as per Matt Pearson's TTC note). Handling of Calibration events during normal running is now being implemented.
A list of low level software needed to exploit these features is being drawn up.
The new Full Debug Tracker header format has been extensively tested and is now standard in V2 firmware. The new APV debug monitoring channel is also working.

The Delay FPGA design has been slightly modified (number of internal DCM steps reduced from 9 to 8) to cure problems observed during automatic timing calibrations. The table relating nsec offset vs skew setting needs to be re-measured and updated, although the change is expected to be small.

The BE FPGA technical description has been updated with full details at
http://www.te.rl.ac.uk/esdg/cms-fed/firmware/Documents/BE_FPGA_Technical_Description.doc
*The full debug information is also provided in VME registers for monitoring (needs testing).

Assembly Plant Testing

Further refinements to the testing plan and LabView application have been made. Testing references have been adapted for Rload=62 Ohm.

A test engineer from eXception EMS will spend a day or two at RAL during the testing of the next batch of 20 boards to gain experience of the procedures.

Final Acceptance Testing

It is proposed that the full crate acceptance tests be concentrated at RAL.
The rack from CERN has been moved (with a little effort) to our lab. Crates have yet to be installed. Solutions for cooling are still being arranged, although cooling is not necessary to start testing.
Missing Equipment. During tracker week Patrice Siegrist told us that we could have the last remaining LHC crate, but it required some repair. Also loan of an adapter for our SBS PCI card was possible. No news of progress on delivery since.
As last resort we may use our test crate temporarily, although it would involve considerable disruption and there is some risk of damage to boards owing to its poor mechanics
Greg is preparing hardware to interface the FED Testers to the TTC system, which will allow multiple FEDs to be triggered.
James is extending the Universal FED tests to permit flexible, multiple FED testing.

Other Items

Numbering Scheme
It is proposed to adopt today a FED channel numbering scheme suggested by Francois.

This has the advantage being unambiguous and still following the optical cabling order.

FE Unit/Ribbon	Fibre	OptoRx pin	DAQ Chan (S/W)	
8	12	F12	812	TOP
8	11	F11	811	
8	10	F10	810	
....				
....				
1	3	F3	103	
1	2	F2	102	
1	1	F1	101	BOTTOM

Final Production:

The DDi Europe group underwent a management buy out effective 9th Feb. The management and technical staff have not changed. The new company agrees to take over all liabilities, contracts etc from DDi. RAL Finance is treating this as a simple change of name.
There has been no disruption of our pre-series production.
(The new group has severed connection with the DDi operations in the USA).
DDi Technologies (Assembly) Calne becomes eXception EMS Ltd
DDi Tewkesbury (PCB) becomes eXception PCB Ltd

Papers have been submitted for CERN Finance Committee in March.
A follow up meeting with eXception EMS to discuss contract issues is now proposed for soon after the CERN Finance committee decision. Meeting to be held at RAL.

INS procurement office is closing and the storage room will be lost shortly. We would like to move the parts we have in hand for final production to Imperial for safe storage with the OptoRx modules. Other items in FED stock will be moved into storage in our lab.