

## Project Monitor Form

<b>Project:</b> CMS FED	<b>PMF number:</b> 10
<b>Date:</b> Monday 25-February-2002	<b>Sheet:</b> 1 of 2

**News and comment**

**Project Spec v1.0** was signed off by Rob and Geoff Hall at customer meeting last week.

Project Implementation phase started.

*Manufacture:*  
Bob has ordered 1000 off AD8138 ARM.  
Quotes received from Impact Memec on 40K and 2M FPGA parts. 40K not available as commercial samples before April and then 10-12 weeks lead time. 2M not available before March with 10-12 weeks lead-time.

*Front End Module:*  
Chris has produced a first order layout of the OpAmp section and its associated components. It appears to fit satisfactorily. He is now working on adding ADC to the layout.

James has modified the VREF/CM circuitry. The new design reduces the number of components and should also remove previously reported signal effects seen at certain frequencies. James has started to simulate the new circuit.

CERN have responded to Adam's suggested improvements to the OptoRx module pinout. We seem to be converging on an arrangement satisfactory to both of us (the company designing the ASIC had actually already altered the pinout in a way that approached Adam's suggestions.) Adam will verify with Francois the extent of de-coupling on the OptoRx module itself (c.f. ASIC.)

*Firmware:*  
Delay FPGA:  
Ed has fitted his full design on the evaluation board (uses engineering sample FPGA.) He will make a more quantitative measurement of the response to phase adjustment settings. Ed is also finalising the pinout for Adam.

*Board level:*  
Saeed has updated the table of current requirements for FED with estimation for FPGA consumption (based on VirtexE simulation.)

*Other Issues:*  
James, Adam, Saeed and Chris should review design progress this week in Rob and John's absence.

Actions from the previous PMF			
Action	Status	Who	Target date

Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	In progress	EF/RH	31-02-02
Produce pinout of Delay FPGA for inspection by Adam.	In progress	EF	11-02-02
Specify board level voltage and current requirements.	Done.	ST	
Make request to R. Stephenson to borrow simulations tools license for James's PC.	On going	RH	11-02-02
Produce proposal scheme and devices for temperature monitoring of OptoRx and FPGAs.	In progress	JS	04-03-02
Produce 1 <sup>st</sup> order FE module analogue component layout.	Opamp section done. Remainder ongoing.	CD	25-02-02
Request quotes from Impact for 1.5 and 2M FPGA parts.	Done.	RH	25-02-02

<b>Actions outstanding and new actions</b>		
<b>Action</b>	<b>Who</b>	<b>Target Date</b>
Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	EF	04-03-02
Produce pinout of Delay FPGA for inspection by Adam.	EF	04-03-02
Make request to R. Stephenson to borrow Orcad professional simulations tools license for James's PC.	RH	11-03-02
Produce 1 <sup>st</sup> order FE module analogue component layout.	CD	04-03-02
Produce proposal scheme and devices for temperature monitoring of OptoRx and FPGAs.	JS	04-03-02
Find out from Paul Hardy whether it is possible, and if so how, to automatically generate Xilinx FPGA symbols in CADENCE.	RH	11-03-02

**Project Monitor Form- milestones**

<b>Project: CMS FED</b>		<b>PMF number: 10</b>		
<b>Project Manager: R. Halsall</b>		<b>Sheet: 2 of 2</b>		
<b>Date: Monday 25-February-2002</b>				
	<b>Milestones</b> from <b>Project Management Plan Version:1.0</b>	<b>date due</b> <b>in PMP</b>	<b>predicted</b> <b>date</b>	<b>date</b> <b>done</b>
1	User Requirements Document	30-07-01		26-09-01
2	<b>Project Spec sign off</b>	<b>21-12-01</b>		<b>05-02-02</b>
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	11-03-02	
5	FE Module Feasibility Review	28-02-02	11-03-02	
7	<b>Board Level Feasibility Review</b>	<b>04-03-02</b>	<b>08-04-02</b>	
8	Delay FPGA Interim Review	31-01-02	04-03-02	
9	Front End FPGA Interim Review	31-01-02	04-03-02	
10	Back End FPGA Interim Review	31-01-02	25-03-02	
11	VME FPGA Feasibility Review	28-02-02	25-03-02	
12	Clock FPGA Feasibility Review	28-02-02	25-03-02	
13	Release Test Plan Document	22-02-02	08-04-02	
14	FE Module Final Review	30-04-02		
15	BE Board Final Review	10-05-02		
16	Full Board Design Final Review	31-05-02		
17	<b>IDR Customer Production sign off</b>	<b>10-06-02</b>		
18	<b>Batch 0 (2 off) Non-Opto Assembled boards at RAL</b>	<b>26-07-02</b>		
19	OptoRx for Batch 0 at RAL	26-08-02		
20	<b>Batch 0 Opto Assembled boards at RAL</b>	<b>01-11-02</b>		
21	Batch 0 review	06-01-03		
22	<b>Batch 1 (8 off) Assembled boards at RAL</b>	<b>21-03-03</b>		
23	<b>Delivery Batch 1 to CERN completed.</b>	<b>11-07-03</b>		