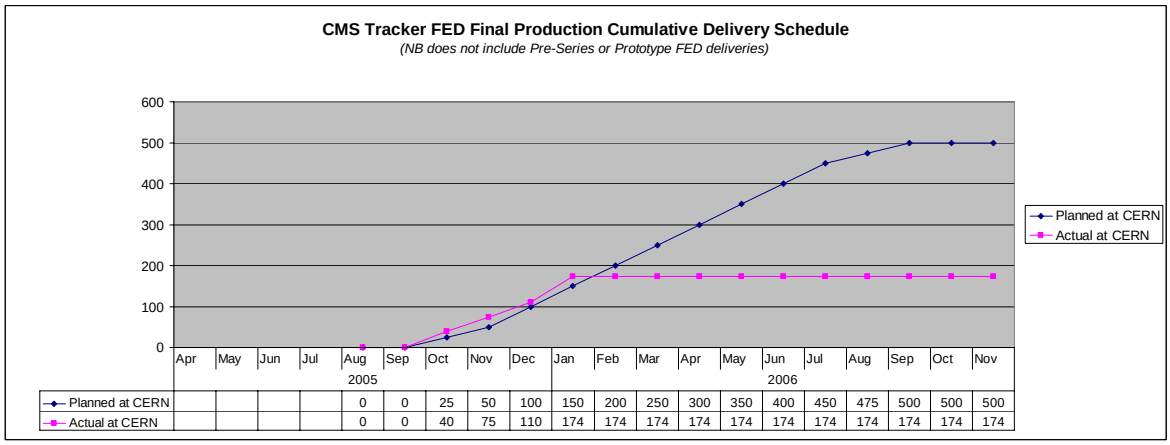
Project Monitor Form

Project: CMS FED **Date:** Wed 25 Jan-2006	**PMF number: 59** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

Board Deliveries to CMS: Remains on schedule.
4nd batch of 64 arrived at CERN last week bringing total to 174 boards.
Next batch of ~ 64 for CERN ready soon.
New arrangement for air freight delivery used for last 2 batches worked well.



	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov
	2005									2006										
Planned at CERN					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
Actual at CERN					0	0	40	75	110	174	174	174	174	174	174	174	174	174	174	174

Production:
Assembly plant test setups working well. Only minor problems quickly resolved….
Linux (Konqueror) browser used to display test results files broke (not understood). This didn't stop testing. Later moved them to alternative browser.
Loop back card came loose which caused constant Bscan errors.
Occasionally visits to help out with a few boards failing tests there.
Need to back up Test Results again soon.

ORx
Final batch of 705 ORx were sent from Imperial to eXception 11 Jan.
Still waiting for stock numbers from eXception. We estimate they have enough for ~ 467 boards.

How to complete production…
Identify any spare stock. 32 at RAL.
Further 120 on order from CERN.
Recover from prototype FEDv1 (~16 boards, incl. 6 duff boards). Return (unused) FEDv1 from CERN.

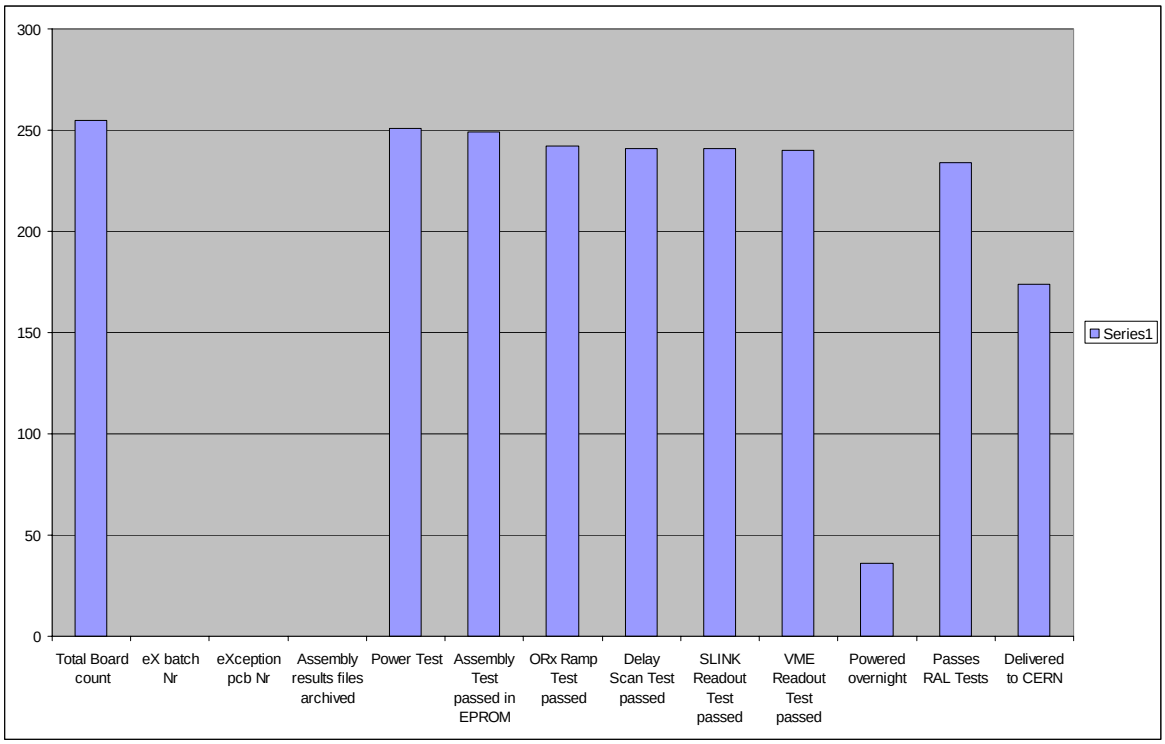
End of year Production review was held at eXception in December.
Reviewed procurement, manufacture, test. No major problems. Keeping to ~ 50 boards per month.
They are experiencing some contractural difficulties with new Xilinx distributor. But this will not affect our production schedule.

SLINK Transition Card production is still on hold until tested with FMM. Order needs to be placed within next 2 months to allow for sufficient testing time.

Testing at RAL:

Catching up with board deliveries from eXception over New Year.

Board quality arriving at RAL still good.
250 boards have now being tested at RAL.



More details are in Production spreadsheet.

Found a temporary fix for odd word swapping effect reported in VME readout on a handful of (BE FPGA firmware update). This allowed Assembly Test to be completed (successfully) on these boards.

CERN Integration :

Tests with final TTC cards (TTCci) in progress.

FMM card throttle test needed before remaining 400 Transition Card production. Probably done at Cessy.

Debugging full rack (3 crate) system in progress. Need to plan for RAL assistance.

Water cooling has failed at 904 (more than once). Fortunately firmware triggered overtemp shutdown of FEDs was introduced for full crate testing!

ADCs should now be disabled outside data acquisition runs.

First production boards have gone to B186 for Tracker Integration.

Firmware :

Some final checking needed on VHDL (Fake Frame) before standard FE FPGA release (see Oz slide). Simple mod was made to allow fake frames to run at full luminosity trigger rates (i.e. back to back frames).

VME BLT readout now stable with CAEN (as of VME 21000327). At limit now (~ 12 MB/sec for 32KB transfer size) without a significant redesign.

BE FPGA fix for word swapping effect (only affected few boards). Need to try with DCM reset code from GCT. Possibly a problem with some DCMs in some FPGAs? Don't want to risk rework to prove this yet.

Request for additional DAQ info word in header (Rob)?

Add a test register for generating Throttle signals (expected needed for FED-FMM validation).

SPY channel capture of Frames. Delay FPGA part to complete (not urgent).

Software:

TTC integration (see above).

Optimising FED parameter loading.

Low level Software status (report by Jo).

fedDebug code put in cvs repository.

Other Items:

Placed order for final 22 LHC crates. Same spec as before. Next delivery due around June, assume would have in hand by September.

Electronics Test lab at RAL is being taken over by Space Science. FED test area will remain until end of 2006.

All TTCoc Front panels now sent to Jan. Jan will takeover design files if further needed.

The Compact Flash cards we use have been rebranded.
eXception are being nominated for CMS Industry award.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Test ZS lite firmware.	Simple test done.	JC	
Update Transition Card BOM.	Awaiting FMM test	ST	28-10-05
Attend CERN Safety Training	JC still to do	All	28-10-05
Carry out end of year review at eXception	Done	JC	
Test DCM firmware from GCT group	Discussed with Dave Newbold	ST	
Contact Attila to arrange FMM tests	Earliest test in February	JC	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Update Transition Card BOM.	ST	01-03-06
Test DCM firmware from GCT group	ST	01-03-06
Attend CERN Safety Training	JC	23-12-05
Return FEDv1 to RAL	OZ	01-03-06
Confirm ORX numbers	JC	01-02-06
Send TTCoc files to Jan Troska	IC	01-03-06

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 59**		
Project Manager: J. Coughlan **Date:** Wed 25 Jan-2006		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05	22.07.05	28.07.05
33	Production of 500 FEDv3 starts	08.09.05	27.07.05	01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05	30.10.05	27.10.05
35	First FED installed at USC55	17.11.05	01.05.06	
36	Last FED installed at USC55	26.07.06	31.09.06	
37	Power on Tracker	01.08.06	30.11.06	
38	Readout test with Tracker	01.10.06	01.02.06	
39	LHC test run	02.04.07	01.07.06	