Project Monitor Form

Project: CMS FED	**PMF number: 34**
Date: Thursday 24 July-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

28 cards passing tests were collected at CERN on 18.7
Remaining 12 failing tests will not be worked until after the holidays at earliest.

FEDv1:

Manufacture

005 with 8 OptoRx (old version) delivered to RAL on Monday 30th June.
003 and 004 (latter with assembly completed after fixing gash) delivered on Monday 30th June.

Necessary mods made before powering boards.
Boards power ok in crate, but some problems powering on the bench. Need to power on bench to use VME Extender cards for loop back tests. Eventually got it working after relaxing current limits on FET controllers. Problem on 12 V bench supply?

JTAG Boundary Scan tests passed with a few minor problems only (Nb BSDL files needed changing for XC2V1500's.)
Solder bridges on Resistor packs between ADCs and Delay FPGA. Need to fix on FEDv2 eg change solder masks.
003 had an LM82 on wrong.
004 (board with gash) had DAC on wrong and 1 J0 pin shorted.
Nb No faults reported on any BGAs on first 5 boards.

004 is now being used for James tests of power circuitry.

Meanwhile Matt reported some further solder bridges on 001 (inaccessible to JTAG.) Also 1 dud DAC channel.

Matt also discovered peaking caps were fitted despite assembly instructions saying not to do it. Investigating how it happened. Partly our fault for not spotting on first pair.
These caps were an option requested at short notice by Francois when settling time problems were being observed on OptoRx. 1 per FE channel, 10pF 0402.
Present on primary side on 001 and 002 . On both sides of 003 and 005 (and probably 004.) Need to remove them.

Request put into Drawing Office to make a further 6 FEDv1 PCBs with no layout changes.
Job pending, awaiting results from Atlas 9U and Daresbury 12U PCBs using tin finish rather than gold. If assembly is ok will use the same on FEDs. Tin should give better long term stability for surface mounted components.

49 more OptoRx (new version with settable caps) received on 21st July.
Jan Troska states that there should be no difference for Large Scale Assembly tests if using old cf new OptoRx.

Proposal for 3 fully assembled FEDs with OptoRx 001,003,005:
Fully assemble 001 with 6 more old version OptoRx. (Exchange it at IC with 003?)
Assemble 003 with 8 new OptoRx.
001 stays in UK, 005 and 003 to LSA/CERN.

Concern: Shortage of TrueLight pin diodes for TTCrx. We had 2 (maybe 3?) from Bruce Taylor. 1 is on 001. We only need 1 or 2 more. CERN Microelectronics apparently due to make a bulk order soon?

Firmware

FE-FPGA:
Reasonable progress made. Including understanding operation of Bill G's design.

Testing Frame Finding mode using simple APV pattern generator in BE test design which feeds by cable from test pin to Electrical test card inputs on all channels of one FE module. We can also adjust data level within frame w.r.t. to header level.
Frame finding is partly working. Evidence that ChipScope was affecting behaviour of design.
Observe 11 out of 12 channels locking to ticks reliably.
Observe correct data length value for event from FE fifos.
Observe stable pipeline address and correct status info bits for 11 out of 12 channels.
Last channel has error bits indicating out of sync. Doesn't recover on DAC reset (other channels do.)
Needs more work to get clean data transfer in test design. Currently data contents are not yet as expected, DDR in test design needs tuning, so may jump to final BE design for further tests.

Need to verify entire complete design in XC2V1500. And modify if necessary.

BE FPGA:
Concentrated effort on this. Very good progress made.

Using Chipscope now observe correct FE data entering and leaving QDR memories (at least for a few triggers.) Timing is quite critical. Hence have moved clock selection logic to VME to free up clock resources in BE.

DAQ and Tracker headers/trailers (including updated DAQ trailer) are also now appended correctly. Data and controls on output lines to V-LINK appear to be ok.

Now adding software serial control registers and some further steering features. Eg ability to disable complete FE modules, ID registers, counters for diagnostics, adding more info to tracker headers…) This involves porting some Verilog code from FE FPGA.
Full register map for BE available in next few days.

So far all tests have used Scope mode triggers. We will add APV test pattern generator to this