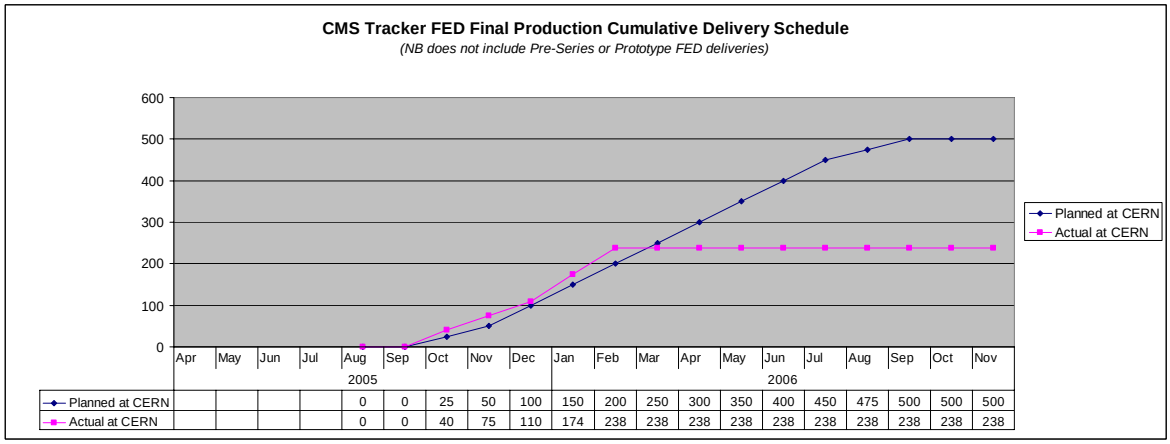
Project Monitor Form

Project: CMS FED **Date:** Friday 24 Mar-2006	**PMF number: 60** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

Board Deliveries to CMS: Remains on schedule.
Total at CERN is now 238 boards.
And another batch of ~ 64 was shipped yesterday.



	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov
	2005									2006										
Planned at CERN					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
Actual at CERN					0	0	40	75	110	174	238	238	238	238	238	238	238	238	238	238

Production:

Proceeding to plan. Expect last assembly run in April/May.
All free issue parts to complete production now with eXception, incl TTCrx. (except ORx see below)

Minor problems in Assembly Test. html file generation was upset by inadvertent characters in some text boxes. Doesn't stop testing. Will fix files retrospectively later.
Occasional visits to help out with a few boards failing tests there.

Testing at RAL is keeping pace (just).
More details are in Production spreadsheet.

ORx

eX are now short of 325 pcs for final assembly run ~ 40 boards.

Unfortunately the final batch of new Opto's (120 pieces = 15 board's worth) from Geneva are delayed and will not arrive before May?
But we do have in hand some Opto's which can be recovered from existing FEDv1 prototype boards.
We have about 30 pieces which are already removed. We plan to send the remaining prototype boards to eX to remove the rest.
This should give us about another 10 board's worth.
That leaves about the final 15 boards out of 500 that we will not have Optos for.

Boards for which Optos are unavailable should still go through all the test procedures at eX.
All tests BScan , VME except for the last analogue test ought to pass as normal. Some boards could be kept until the new batch of Optos do arrive and can then be assembled and final analogue test completed.
Leaving 15 unpopulated boards we will accept as long as they pass all the other tests. SLINK could be

tested with Fake Frames.

SLINK Transition Card

Basic connectivity tests with FMM with slow throttle signals at 904 over a weekend were successful. Remaining 430 boards have now been ordered. Expect back in May. Then need testing at RAL.

Only change from first 70 cards is RJ45 (cable to FMM) replaced by shielded connector. This can be linked to Gnd point on card if it proves necessary, but it won't be done otherwise.

CERN Integration :

Vertical slice Tests of FEDs with final TTC cards (TTCci) and FEC working.
Tests with APVe also started. Still to do with FMM fast throttle.

Tests of 16 FEDs to FRLs in mobile crate in progress. Single links working. Merged links giving errors (at low rates?)

Rack mounted PCs installed with crates in B904. See Rack layout diagram from Oz.

Racks in place for production boards at B186 for Tracker Integration. Expect to move large nr FEDs in March?

Adding VME J0 backplane cards to 904 crates for multiple VME FPGA reprogramming as for Pt5 final system.

Firmware :

FE VHDL Psedo Random data added to Fake frames.

Observed some odd behaviour with setting of some FE registers eg Super mode takes 2 attempts? Could be fedDebug software. Look with Chipscope.

BE will add additional DAQ info word in header.

BE Added test register for generating Throttle signals (used for FED-FMM validation).

BE fixed header store of changing PipeAddrs (simple bug was introduced when we added Fake modes)

Fast Init added to VME.

New VME 2100032B as standard relase (needed for Compact Flash reprogramming via VME using CAEN)

SPY channel capture of Frames. Changes for Delay FPGA is next task at RAL.

Software:

Fast Pedestal loading with multiple serial commands and BLT writes is working.

Low level Software status (see report by Jo).

Standalone utility for reprogramming CFlash over VME being developed at RAL. fedDebug tool does it now.

Other Items:

Half of electronics Test lab at RAL is being taken over by Space Science.
FED test area is being slightly rearranged, but will remain in place until end of 2006.

PPARC commissioned photographer spent a day in RAL test lab. Photos available.

eXception visit to CERN to collect CMS Gold award went very well. Photos available.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Update Transition Card BOM.	Done	ST	
Attend CERN Safety Training	JC still to do	All	28-10-05
Contact Attila to arrange FMM tests	Test Done	JC	
Return FEDv1 to RAL	Done	JC	
Confirm ORX numbers	Done	JC	
Send TTCoc files to Jan Troska		IC	01-05-06

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Attend CERN Safety Training	JC	01-05-06
Send TTCoc files to Jan Troska	IC	01-03-06
Order shielded RJ45 for existing Transition cards	IC	01-05-06
Get parts to install J0 backplane cards at CERN	IC	01-05-06
Implement SPY mode in Delay FPGA	ST	01-06-06
Implement additional status word in BE header	ST	01-06-06
Fix html files at eXception	JC	01-06-06

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 60**		
Project Manager: J. Coughlan **Date:** Friday 24 Mar-2006		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05	22.07.05	28.07.05
33	Production of 500 FEDv3 starts	08.09.05	27.07.05	01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05	30.10.05	27.10.05
35	First FED installed at USC55	17.11.05	01.05.06	
36	Last FED installed at USC55	26.07.06	31.09.06	
37	Power on Tracker	01.08.06	30.11.06	
38	Readout test with Tracker	01.10.06	01.02.06	
39	LHC test run	02.04.07	01.07.06	