Project Monitor Form

Project: CMS FED	**PMF number: 35**
Date: Friday 22 August-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FEDv1:

Manufacture

Manufacture of a further 6 FEDv1 PCBs given go ahead. No layout changes.
(Using Tin finish like Atlas boards which just passed Boundary Scan tests.)
Expect bare PCBs back 2nd week September.

Further tests of power circuitry carried out on 004. Improving protection circuitry on QDR power supplies. Suggestions for better FET controllers. Plus some other changes which will be made and tested on CALICE boards.
James is moving to another project soon. Work is being handed over to Ivan.

Need to improve communication of assembly instructions. Lessons from inadvertently fitted peaking caps.
Last set of assembled boards.
Have tested 003 (without OptoRx) in crate. Next test 005 (with OptoRx).
NB FE FPGA full design fitted in XC2V1500. Encouraging. Needs more exhaustive testing.

Need to fully test 005 optically. First board for delivery outside UK.
Then assemble 003 with 8 OptoRx.

TrueLight pin diodes for TTCrx. CERN MicroElectronics responsible for bulk LHC orders. None from CMS. We got last device from Sandro in hand. We have put our own small (25 off) order in to Taiwan. Atlas have tried but failed to get some already.

Firmware

All functionality needed for LSA tests, except for TTC clock and trigger, have been tested at RAL in standalone setups and with standalone software (cf Imperial system tests with final software and external signal sources).

FE-FPGA:

In good shape.

Fixed problem in DDR input block (which was causing odd structures in sine wave captures.)
Lack of convenient visualisation tools hampered studies. Using tcl scripts and Excel to do it.

Further tests of Frame Finding have been made and it seems to work.
Verified pipe address readout and apv status bits. Locking to ticks and frames.
Can do simple things in our standalone loop back setup. Need better control of input rates/data

patterns. Found out what happened when FE buffers overflow!

Checked full final design “places & routes” in smaller XC2V1500. Scope mode seems to work.

Discovered a few more features of the design. ADC settings don’t seem to read back properly.
Presence of ChipScope definitely seems to screw up aspects of operation of logic.
(All official releases of all FPGA final firmware will have ChipScope cores removed.)

BE FPGA:

Excellent progress was made. Design needed for LSA implemented and fundamentals tested before Saeed left on vacation.

A full set of registers for control and monitoring logic operation from VME were added as needed for LSA tests.
Plus some extra features. FE data lengths added to header. Ability to ignore data from selected FE FPGAs. Flags to indicate status of buffers. Firmware revision register.

Building of events with FE data in scope mode and frame finding tested (latter done by adding apv frame generator from test design.)
DAQ headers/trailers and Tracker headers verified for a few events. Need final software readout for more exhaustive testing.

VME FPGA:
Major progress made.

VME event readout is now working.
Temporary restriction that event < 32 KB buffer (not a problem for Imperial tests).
Otherwise all features needed for LSA tests done.

External clock selection is implemented. Backplane clock tested.
Full FED reset over VME implemented. Firmware ID register.

Bug found in VME FPGA operation during Imperial tests manifesting as long delays between VME bus cycles. Traced to mis-assignment of DTACK buffer enable pin. We introduced it when including Matt’s improvement to DTACK logic a few weeks ago. Now fixed.

<u>Other Work</u>
TTC:
Tests with TTCrx have not succeeded yet. Currently using Backplane clock/trigger as external source.
Have setup TTCvi and TTCex at RAL. Spent some time understanding operation of TTCrx.
Suspect that BE FPGA is not resetting TTCrx correctly.
This is the last function we need working for LSA tests.

S-LINK:
Eventually obtained the pin out of ECAL Transition card for S-LINK PMC. It is possible we could use it for FED kit tests with some minor mods.