

Project Monitor Form

Project: CMS FED

PMF number: 56

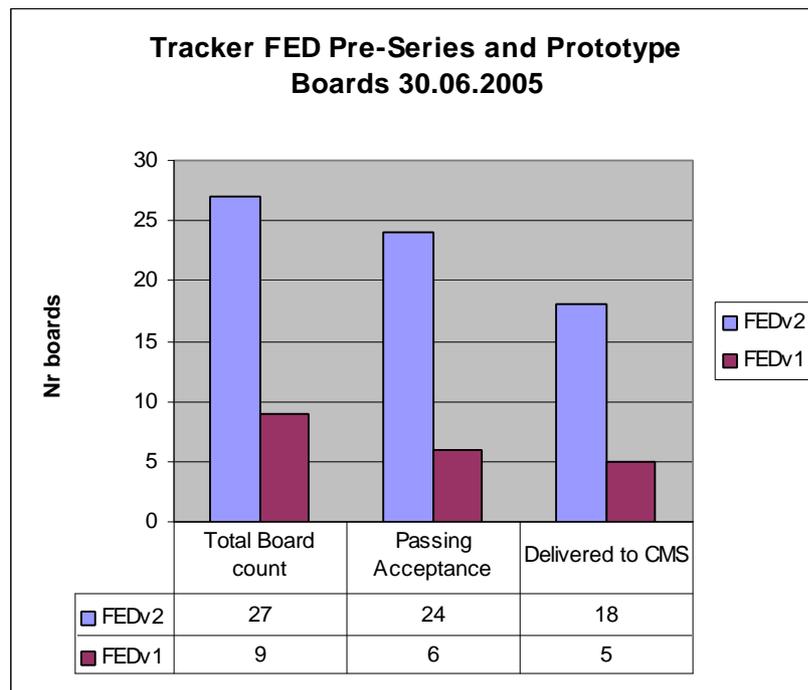
Date: Friday 22 July-2005

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Project Implementation phase.

Pre-Series FEDv2

Another 10 pre-series boards shipped to CERN since last meeting as agreed.
Loaded with ACE 06_05_05 ; VME 21_03_1D



Production FEDv3

Design files were reviewed and all minor mods introduced since FEDv1 updated on schematics (e.g. component value changes).

Only change DC-DC converter holes on pcb increased slightly.

Production boards will be revision FEDv3 (PC3205M/3). But it is the same design as pre-series FEDv2. Board serial nrs carry on from pre-series.

First 2 production LHC 9U crates (final PS, larger fan trays) were delivered to RAL on 29.6
One was exchanged with FED crate in RAL rack.

Took second SBS VME bridge from Imperial for Assembly test.

New PCs arrived for Assembly tests.

2 crates were collected by eXception for our Test Setup on 11.7, together with production quantities of RAL free issue components (except ORx enough for 100 boards).

Boundary Scan and LabView Test Kit installed at eXception on 19.7.

LabView working, Bscan needed some adjustments, but now ok.

First batch of 50 boards.
ORx are being machine assembled.
First 2 boards were in conventional assembly Wednesday and due to be ready for test by today.
Allow 2 working days for test before completing assembly of remaining 48 boards.
Aim is to have 50 boards delivered to RAL by end of August.

Transition Card

Design files were handed over to RAL after last meeting.
Job was put out direct rather than through Drawing office.
Quotes were obtained. Production to be done by Cemgraft. PCBs from Express as before.
1st batch of 70 boards are expected by end of July. Do 2nd batch of 400 after these are tested.

Other Activities:

Quote for RAL Rack cooling accepted. Expect to be installed before end of August.

Tracker DAQ systems moved to B904.

During recent Tracker week first 3 boards (18, 19, 24) sent to CERN had power mod done.
3 FEDv1s (3, 15, 16) were upgraded to FEDv2 firmware.
There is a shortage of SBS cards (4 stopped working) so use of CAEN becoming necessary.
CAEN brought to RAL this week for BLT tests.

Sandro Marchioro spent a day at the FED lab end June to see set up for FED acceptance tests.

Design Testing :

Several clock timing measurements repeated on FEDv2s. Request from Karl Gill.
TTCrx output spread < 800 psec.
TTCoc < 800 psec
Spread channel to channel on FED < 400 psec.
Delay vs skew setting updated table.

Firmware :

VME FPGA:

Fixed clock swapping problem with CAEN CC. Block Transfer now working with CAEN CC.
Block Transfer errors with SBS being investigated.

FE FPGA:

Fake Frame generator is now tested and working with debug software. Other FE functions seem to be working in this VHDL version. Final software under development to exploit in Tracker DAQ. Needs further exercising in final systems at CERN before we switch to Osman's VHDL version as default release.

New ZS-Lite mode is implemented and ready for testing.

BE FPGA

Fixed J0 throttle problem. It was being disabled if Transition card not present.

Contracts:

The contract with eXception EMS was signed last week of June. The corresponding Purchase Order was placed. The project code for payments for production is ready.

RAL amendments to the draft Agreement with CMS were sent to CERN at 8th June Payment schedule is in £ sterling. Document is still awaiting signature by CERN management.

Actions from the previous PMF			
Action	Status	Who	Original Target date
Order chiller unit	Done.	IC	
Stock check and spreadsheet of remaining FED components	Partially done. Free issue sent to eXception..	IC	
Arrange for signing contract with eXception	Done.	JC	
Obtain quotes for Transition card production	Done	ST	
Obtain 2 9U crates for Assembly tests	Done	JC	
Obtain PCs for Assembly tests	Done	IC	
Fix remaining pre-series boards		IC	30-06-05
Complete route cards for pre-series	Done for shipped	IC	
Ship 10 more pre-series boards to CERN	Done	IC	

Actions outstanding and new actions		
Action	Who	Target Date
Fix remaining pre-series boards	IC	31-07-05
Get Test kit running at Assembly plant.	IC	22-07-05
Fix Block Transfer firmware.	ST, EF	31-07-05
Test ZS lite firmware.	JC	31-07-05

Project Monitor Form- milestones

Project: CMS FED		PMF number: 56		
Project Manager: J. Coughlan				
Date: Friday 22 July-2005		Sheet: 2 of 2		
	Milestones from Project Management Plan Version:1.6	date due in PMP	predicted date	date done
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05	22.07.05	
33	Production of 500 FEDv3 starts	08.09.05	27.07.05	
34	First FEDv3 at B904 Preveessin	30.11.05	30.10.05	
35	First FED installed at USC55	17.11.05	01.03.06	
36	Last FED installed at USC55	26.07.06	31.09.06	
37	Power on Tracker	01.08.06		
38	Readout test with Tracker	01.10.06		
39	LHC test run	02.04.07		