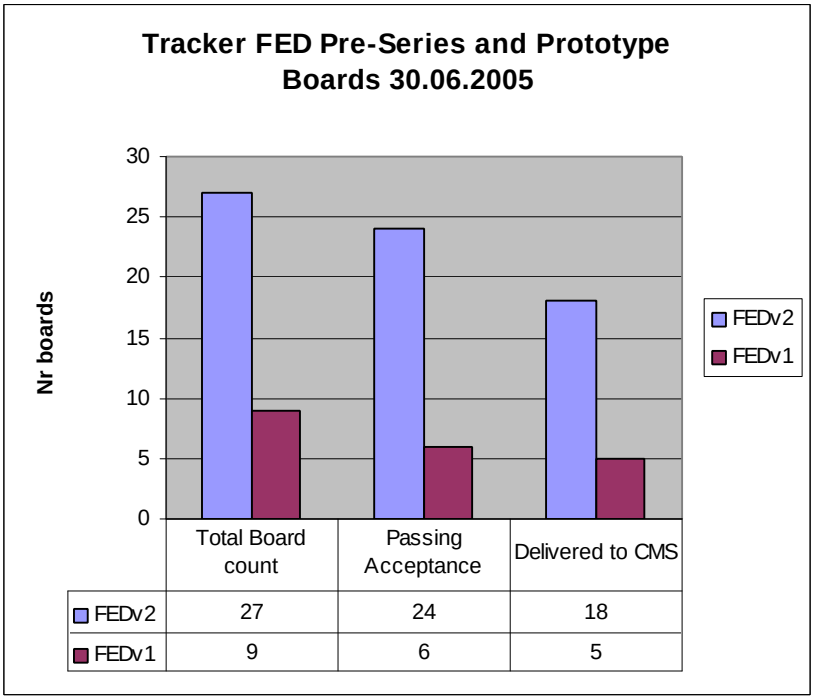
Project Monitor Form

Project: CMS FED **Date:** Friday 22 July-2005	**PMF number: 56** **Sheet:** 1 **of** 2

Project Implementation phase.

Pre-Series FEDv2

Another 10 pre-series boards shipped to CERN since last meeting as agreed.
Loaded with ACE 06_05_05 ; VME 21_03_1D



Production FEDv3

Design files were reviewed and all minor mods introduced since FEDv1 updated on schematics (e.g. component value changes).
Only change DC-DC converter holes on pcb increased slightly.
Production boards will be revision FEDv3 (PC3205M/3). But it is the same design as pre-series FEDv2. Board serial nrs carry on from pre-series.

First 2 production LHC 9U crates (final PS, larger fan trays) were delivered to RAL on 29.6
One was exchanged with FED crate in RAL rack.
Took second SBS VME bridge from Imperial for Assembly test.
New PCs arrived for Assembly tests.

2 crates were collected by eXception for our Test Setup on 11.7, together with production quantities of RAL free issue components (except ORx enough for 100 boards).

Boundary Scan and LabView Test Kit installed at eXception on 19.7.
LabView working, Bscan needed some adjustments, but now ok.

First batch of 50 boards.
ORx are being machine assembled.
First 2 boards were in conventional assembly Wednesday and due to be ready for test by today.
Allow 2 working days for test before completing assembly of remaining 48 boards.
Aim is to have 50 boards delivered to RAL by end of August.

Transition Card

Design files were handed over to RAL after last meeting.
Job was put out direct rather than through Drawing office.
Quotes were obtained. Production to be done by Cemgraft. PCBs from Express as before.
1st batch of 70 boards are expected by end of July. Do 2nd batch of 400 after these are tested.

Other Activities:

Quote for RAL Rack cooling accepted. Expect to be installed before end of August.

Tracker DAQ systems moved to B904.

During recent Tracker week first 3 boards (18, 19, 24) sent to CERN had power mod done.
3 FEDv1s (3, 15, 16) were upgraded to FEDv2 firmware.
There is a shortage of SBS cards (4 stopped working) so use of CAEN becoming necessary.
CAEN brought to RAL this week for BLT tests.

Sandro Marchioro spent a day at the FED lab end June to see set up for FED acceptance tests.

Design Testing :

Several clock timing measurements repeated on FEDv2s. Request from Karl Gill.
TTCrx output spread < 800 psec.
TTCoc < 800 psec
Spread channel to channel on FED < 400 psec.
Delay vs skew setting updated table.

Firmware :

VME FPGA:
Fixed clock swapping problem with CAEN CC. Block Transfer now working with CAEN CC.
Block Transfer errors with SBS being investigated.

FE FPGA:
Fake Frame generator is now tested and working with debug software. Other FE functions seem to be working in this VHDL version. Final software under development to exploit in Tracker DAQ. Needs further exercising in final systems at CERN before we switch to Osman's VHDL version as default release.

New ZS-Lite mode is implemented and ready for testing.

BE FPGA
Fixed J0 throttle problem. It was being disabled if Transition card not present.

Contracts:

The contract with eXception EMS was signed last week of June. The corresponding Purchase Order was placed. The project code for payments for production is ready.

RAL amendments to the draft Agreement with CMS were sent to CERN at 8th June Payment schedule is in £ sterling. Document is still awaiting signature by CERN management.