Project Monitor Form

Project: CMS FED **Date:** Thursday 22 April-2004	**PMF number: 45** **Sheet:** 1 **of** 2

Project Implementation phase.

FEDv1:

FED Status:

All analogue channels on all 6 new boards are now working.
Minor repairs were needed on some channels. Usually hand soldered term resistors or DAC pins.

Comprehensive production report received from DDi.

Nr 14 sent to CERN on 2nd April.

Occasional problems with TTCrx reset finally identified. Due to misunderstanding of document. JTAG Reset line was tied high instead of low. Simple hardware fix, which has been done on all boards at RAL.

System Tests

Operation with TCS throttle signals @40MHz verified at Imperial

Temperature tests show OptoRx and ADCs running hot.
Fan tray positioning in our crates is far from optimal. Plan to test in Atlas crate with 9 x fan tray. Need to investigate other measures.

FEDv2

Draft FEDv2 schematics completed, but still to be reviewed.

PCB layout changes in preparation.
Darren Ballard will carry out the work, as Chris Day is likely to be occupied with Atlas job for several weeks.

Replacement for QDR identified. Samples on order.
Decision to change package or buy up VREF to be made soon.
VME EPROM JTAG programming lines to be brought to J0 with cable chained on back plane. Reprogram from laptop or permanently mounted PC.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Sign off new project deliverables with customer.		JC	26-03-04
Test next 6 FEDs	Done.	IC/JC	
Send 2 new FEDs to CERN.	Done.	JC/IC	
Hold washout review with DDi.	Done.	JC/IC	16-04-04
Complete FEDv2 schematics.	First draft Done.	ST	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Sign off new project deliverables with customer.	JC	03-05-04
Hold washout review with DDi.	JC	03-05-04
Make first release of FEDv2 layout.	DB/ST	03-05-04
Repeat temperature measurements in ATLAS crate.	ST/JC	30-04-04

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 45**		
Project Manager: J. Coughlan **Date:** Thursday 22 April-2004		**Sheet: 2** **of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		
27	FEDv2 tape-out	16.07.04		
28	First FEDv2 boards at RAL	08.10.04		
29	Dispatch calls for Tender	26.08.04		
30	Award Tender contract	09.02.05		
31	FEDv3 tape-out	06.04.05		
32	First FEDv3 boards at RAL	13.07.05		
33	Production of 500 FEDv3 starts	08.09.05		
34	First FEDv3 at B904 Prevessin	30.11.05		
35	First FED installed at USC55	17.11.05		
36	Last FED installed at USC55	26.07.06		
37	Power on Tracker	01.08.06		
38	Readout test with Tracker	01.10.06		
39	LHC test run	02.04.07		