

Project Monitor Form

Project: CMS FED Date: Thursday 21-November-2002	PMF number: 20 Sheet: 1 of 2
<p>Project Implementation phase.</p> <p>News and comment</p> <p>Schedule: About 1 week was needed to implement changes from Final Review (see below). Component changes, layout mods and Power plane changes.</p> <p>Routing now back in progress. Updated schematics with final titles produced.</p> <p>Expected Tape (from PMF 19) out was Week 46. In addition Chris is currently off sick with flu. Revised Tape out now expected in week 48.</p> <p>Personnel: Request has been made for Ivan Church (ESSG) to join the project as Test Engineer. Starting Dec->Mar @30% and ramping up effort thereafter.</p> <p>Staff Effort: An external review (made up of RAL/International panel) of all TD effort for Atlas and CMS during the remainder of the construction phase (up to end of FY 06/07) was held (at rather short notice) on 14th Nov. The profile of the effort for the FED was adjusted (see spreadsheet doc CMS-FED-004 Oct02) to match the updated FED production and installation schedules. The total effort of 22.3 SY (FY 02/03 -> FY 06/07) matched that given in the CMS mid term review document presented to the PPRP. The revised profile assumes that unused effort from the previous and this FYs can be carried over. It was stressed at the review that the effort profile has no contingency whatever.</p> <p>Manufacture: Assembly company selected is SAE Tech. They now have machines for automated BGA assembly (although they may not be used for first pair of FEDv1s). Parts list has been sent to SAE Tech. They confirmed it as readable. Assembly company SAE Tech preparing for job. Parts list sent. Placement list to do later. Europractice looking at generation of ODB++ files (in addition to Gerber) for PCB company. Might speed up manufacture.</p> <p>Problem: XC2V40 Delay FPGAs : Whilst re-checking kit realised that pack received (some months ago) marked as ES ie Engineering Samples</p>	

We ordered full production parts. Other FPGAs are ok.
ES do not guarantee necessary features for programmable clock skewing
Nb ES was used on development board. And design did appear to work.
Supplier investigating.
Options: Return to check / Get replacements / go ahead with ES and risk / refit later / wait and delay

Procurement for 20 FEDv1:

Quotes for 20 x FEDv1 FPGAs obtained. Longest lead time is 12 weeks.
Target FE FPGA 1500 now £170 (~20% reduction in 10 months).
Requisition for FPGAs for next 20 x FEDv1 sent to procurement. (Nb Total was just over £50 K meaning Lab Directorate signature was required).
ADCs order also sent to procurement.

Precise cost of components for first pair of FEDv1 = £4,600 (excluding OptoRx!)
Cf estimates (based on web pricing etc...) of £4,450
This does not include manufacturing or assembly costs. Quotes still awaited.

Design:

Back end layout was modified to move BE-FPGA as close as possible to S-LINK connector.
Vias around components done.
Detailed routing of FE->BE lines (minimising vias) has been investigated.

An internal Final Review of the board was held on 6th Nov.
Final Internal Review 6th Nov. All Day.
Adam Baird as internal reviewer.

Schematics were approved.
Design was ok. But several minor changes suggested...
Resistor values on JTAG chains.
OptoRx default pull ups.
Moving de-coupling
Afterwards: JTAG power on QDR was changed for 2.5V

Layout:
Originally had 12 layers: 8 signal + 3 power & 1 gnd
Strong recommendation to use 2 Gnd planes.
Problems to split power planes.
Decided to try for simplest option and go to 14 layers (ie + 2 GND) (see below)

Auto routing converged (99%) but didn't do a good job with critical signals...

BE-QDR lines
Clocks LVDS
FE->BE FPGA data lines
S-LINK

Started redoing these by hand.
Need 8 signal planes. BE FPGA area congestion is limiting factor.

Interruptions to investigate going to 14 layers with PCB company.
This solution is ok.

Impedance matching still ok 56 Ohm cf 70 (100 Ohm Differential)
Resistor value changes required.

Track thickness reduction may help with routing.

JTAG chain has been re-checked with Test section.
NB No BSDL file available for TTCrx (must bypass this device).

Testing:

Need at RAL to be able to test analogue circuits of FEDv1 before OptoRx are assembled.
Document describing 2 proposed electrical test cards produced.
Card 1 is simple based on Transformers. Takes input from Signal Generator. Integrity checks.
Card 2 is more advanced with OpAmps, DAC and FPGA. Performance measurements.

Card 1 proved difficult to fit layout for 12 channels.
An intermediate solution between 2 card designs was suggested instead
Uses AD8131 rather than Transformers to generate sine wave signals to FED from Signal
Generator.
Design on hold. To be discussed with designers of IC test board.

Given slippage in FED production we need to see if we can recover time in Test plan.
IC have equipment and personnel waiting and wish to get a board asap.

Firmware & Software:

VME-FPGA:
Basic interface to BE-FPGA done.
Started to implement "engine" in BE FPGA to communicate with FE FPGAs via serial ports.
This translates commands for loading FE registers eg. Peds, Clock skews.
Engines proved more tricky than expected.
So propose to do a lot more of work in software.

Installed CERN Linux. XDAQ installed with help from Matt Noy.

Video conf FED Online S/W meeting at CERN.
First draft of Tracker framework Documentation released by Laurent.

Crates:

FED Crate requirements document was updated.
Refers to Final LHC crate specs document.
Sent to CMS and to LHC crate rep.

Meanwhile for first 2 test systems.
Rob has ordered PSU.
Costas has ordered 21 slot VME64x backplanes. And extender boards.

DAQ:

More discussions have taken place at CERN on merits of DAQ link with PMC and Transition module versus Rob's suggestion to drive cable directly from FPGA.
Our position is that FEDv1 is designed to be able to test both options.

Next RUWG to discuss CRC checking in S-LINK. See Emlyn Corrin's design.

CERN

During Tracker week 43 CMS module testers made a request for 2 FEDv1s to be available for TIB tests as early as August 2003. TIB has special needs in terms of number of channels to be tested that apparently can't be satisfied by PMCs.

It was stressed that this time-scale would be extremely difficult to achieve and could well have a negative impact on the overall schedule. But we agreed to try our best. We requested a list of the exact functional requirements of these boards.

AOB:

A Fibre-Optic Safety Course has been proposed at RAL for Friday 20th December (morning).

Next Meetings:

FED-UK Meeting to concentrate on Testing. Week 48
CMS week 49. Online S/W meeting. RUWG.

Actions from the previous PMF			
Action	Status	Who	Original Target date
Complete FE module routing.	Done	CD	
Final adjustments to Board level layout complete & reviewed.	Done	CD	
Schematics and netlist released.	Done	CD	
Board level routing completed.	Autorouted Done	CD	
FED sign off and out to manufacture.		CD	15-11-02
Review FED memory map.	Done	JC/EF	
Produce FED software driver lib API.		JC	29-11-02

Actions outstanding and new actions		
Action	Who	Target Date
FED sign off and out to manufacture.	CD	27-11-02
Produce FED software driver lib API.	JC	29-11-02
Order DAQ PC	JC	06-12-02

Re-Test Delay FPGA design on XC2V1000C board	EF	22-11-02
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Project Monitor Form- milestones

Project: CMS FED		PMF number: 20		
Project Manager: J. Coughlan		Sheet: 2 of 2		
Date: Thursday 21-November-2002				
	Milestones from Project Management Plan Version:1.3	date due in PMP	predicted date	date done
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02	30.08.02	
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02	08.11.02	
15	Full Board Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off&Board Out	07.10.02	27.11.02	
17	Batch 0 (2 off) Non-Opto Assembled boards at RAL	11.11.02	23.12.02	
18	OptoRx for Batch 0 at RAL	26.08.02		
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.02		
21	Batch 1 (10 off) Assembled boards at RAL	04.07.03		
22	Delivery Batch 1 to CERN start	12.09.03		
23	Delivery Batch 1 to CERN completed.	04.12.03		