

Project Monitor Form

Project: CMS FED Date: Monday 21-January-2002	PMF number: 05 Sheet: 1 of 2
<p>News and comment Feasibility Study continues.</p> <p>The first FED Design meeting was held last Wednesday. Rob gave an overview of the design. Resulting actions were appended to this document. It is planned to hold such Design meetings weekly.</p> <p>CMS-FED Projects QA area has been tidied up. The PMFs are now available from these pages.</p> <p><i>Front End Module:</i> Footprint for OptoRx is done. Symbols for ADC, Opamp already entered. Investigating tools for generating CADENCE symbols for Xilinx FPGAs. James's schematic, entered in Concept, is now being checked by Adam and should be handed over to Chris today. James has obtained access to Pspice tools (John Lipp) to continue with circuit simulation studies.</p> <p><i>Firmware:</i> Using the 40K evaluation board Ed has succeeded in shifting the DCM phase in a controlled fashion over the full 360 degrees using a simple test design. He will now implement this mechanism in his full design.</p> <p>After sorting out some Xilinx COREGEN issues, Saeed has got a simulation model of Azmat's BE FPGA design running on his own PC.</p> <p><i>Other Issues:</i> A request was made for CMS test bench to inherit at least one of Rob's groups old PC's (latter are to be replaced by new machines soon).</p>	

Actions from the previous PMF			
Action	Status	Who	Target date
Produce procurement list for 9U Prototype	Ongoing	JC	17-12-01
Investigate tools to create CADENCE symbols of Xilinx FPGA.	Ongoing	RH	21-01-02
Pass schematic for Analogue part of Front End module to DO	In progress	JS/CD	17-01-02
Test key aspects of Delay FPGA on development board in Lab	In progress	EF/RH	31-01-02
Send Chris pinout of OptoReceiver	Done	JC	
Send Chris VITA specs	Done	RH	

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Actions outstanding and new actions		
Action	Who	Target Date
Produce procurement list for 9U Prototype	JC	31-01-02
Investigate tools to create CADENCE symbols of Xilinx FPGA.	RH	28-01-02
Pass schematic for Analogue part of Front End module to DO	JS/CD	28-01-02
Test key aspects of Delay FPGA on development board in Lab	EF/RH	31-01-02
Obtain assembly estimate for 500 H1FTT (in 9U) as guide of CMS costs.	BT	18-02-02
Look at Temperature monitoring of FE Module (OptoRx/Virtex)	JS	28-02-02
Book cards (9U FED/Test cards) into Drawing Office	JC/RH	28-02-02
Put LHC crate info on web	JC	28-01-02
Specify voltages and current requirements.	RH	18-02-02
Link VITA specs to web	RH/JC	28-01-02

Project Monitor Form- milestones

Project: CMS FED		PMF number: 05		
Project Manager: R. Halsall		Sheet: 2 of 2		
Date: Monday 21-January-2002				
	Milestones from Project Management Plan Version:	date due in PMP	predicted date	date done
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01	31-01-02	
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	31-01-02	
5	FE Module Feasibility Review	28-02-02	28-02-02	
7	Board Level Feasibility Review	04-03-02	04-03-02	
8	Delay FPGA Feasibility Review	31-01-02	31-01-02	
9	Front End FPGA Feasibility Review	31-01-02	31-01-02	
10	Back End FPGA Feasibility Review	31-01-02	31-01-02	
11	VME FPGA Feasibility Review	28-02-02	28-02-02	
12	Clock FPGA Feasibility Review	28-02-02	28-02-02	
13	Release Test Plan Document	22-02-02	22-02-02	