Project Monitor Form

Project: CMS FED	**PMF number: 48**
Date: Tuesday 20 July-2004	**Sheet:** 1 **of** 2

Project Implementation phase.

FEDv1:

Board nr 12 with new QDR memories has subsequently shown a problem on at least one address line. Samsung have informed us that a BSDL file should be available in the "next days" to verify rework of BGAs. Therefore purchase of production quantities (=MoQ) is on hold.

FEDv2

Job for first 2 FEDv2 progressing well. Component kit collected on 7th July. No major queries. Expect boards back in first half of August.

Testing :

Investigating readout format errors observed during beam tests. Can reproduce major effect (missing first data word from FE) with the FED Tester at high rates. Problem is believed to be in clock domains between FE and BE FPGAs. New firmware under test.

Extensive studies of the rare FPGA loading failure affecting some boards. Verified that the JTAG chain (buffering and termination scheme) is good. Changing clocking speed to ACE controller didn't solve effect. Verified that FPGA does actually load correctly in these cases by reading back contents and comparing with master bit file. Problem is in subsequent start up. Trying some suggestions from Xilinx bug pages. Possible solution (new firmware file) being tested.

Firmware :

Need to prioritize firmware tasks for this year. Main effort now is to cure problems for September beam test.

Other Items

10 more FEDv1 Front Panels with Francois.
50 more for FEDv2 (labelled from 1 to 8 (bottom to top) now being made.

Production quantity TTCrx and PIN diodes now at Imperial.

RAL no longer has (ZEUS) water-cooled racks. Request one from CERN for full crate tests.

Transition card will be compatible with both FEDv1 and FEDv2 (by changing resistors on Transition card).

Tender :
Meeting held at RAL on July 16th to discuss issues for FED tender of second stage of RAL general PCB Framework contract. Expect to get firm quotes for board manufacture (excluding custom tests) from this exercise.