Project Monitor Form

Project: CMS FED	**PMF number: 27**
Date: Wednesday 19-March-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

Status:
Tests still proceeding to schedule.

Electrical Tests

James's switch-point test cards are working well. Now routinely used for all electrical tests.
Can drive all 12 channels from single signal generator input. Cross-point switch configuration program running on Tetronix digital scope.
10 test cards available.

If no input to test card it generates a 1V reference which gives approximately half scale pedestal in ADC.
NB Pedestals are much cleaner with test card generated inputs than was observed when driving signals directly onto FED pins. 10 mV noise structure reported previously could have been artefact of test (poor grounding?)
NB Ivan R. has analysed some of the ADC data with Excel tools and made some nice plots.

Checked sine wave input on all channels on the modules to be fitted with OptoRx.
First 11 channels on each module looked ok, but only saw pedestal on last channel? Found that first DAC channel (which actually feeds last ADC channel) was not providing reference voltage.
Discovered that DACs were being held in reset. Cured by sending reset to DAC.

Optical Tests

Ser 001 sent out last week, in accordance with schedule, for assembly of 2 x OptoRx and replacement of QDRs. Expected back today.
(electrical tests continued on ser 002.)

Matt is setting up Opto-Test card bench at RAL to do preliminary optical tests on FED.
Took back NI/VXI cards from PPD.
NB Lab laser safety responsible requires evidence of class 1 laser hazard classification for our test equipment.

Propose one week of optical tests at RAL. Then kit returns to Imperial with FED ser 001.

Digital Tests

Front-End:
Ivan C. has taken over basic test firmware. He is now proficient with the necessary tools.
Have been testing Double Data Rate transfers from Delay to FE FPGAs. Started with final Delay chip design, but could not reconstruct data in FE FPGA (with simple test design in latter).
Went back to simpler counter data generated in Delay. Saw incorrect counter values in FE FPGA. It took a while to understand effects. First due to DCM clock set-up. Need to cascade

DCM resets until previous DCM has locked to clock. Also problems with misinterpretation of order of byte transfer in DDR receiver and allowance for latency in receiver circuit.
But DDR is now working. Testing it with ADC data now.
Next: Try again with Delay chip final design feeding ADC data to FE FPGA.

VME Tests:
Started tests using RIO as master in FED crate. Used PPCMon program on RIO to generate basic VME cycles to FED. Can also do block transfers using BMA engine on RIO. Other debug tools include VMETRO bus analyser, Chip Scope in VME FPGA and VME Extender card (in neighbouring slot) connected to scope.
Tested basic VME Slave interface block with 4K of Block RAM in FPGA. VME address space of FED set to 64KB in A32 space (D32 access only.) Base address is set by geographic address i.e. slot number. NB Block RAM is mirrored 16 times in memory.
Single cycle VME reads and writes are working. All expected AM codes are recognised. (Apparent failure on AM 0D turned out to be bug in PPCMon!) Obtain bus error on non-D32 accesses as expected. Short (30 min) soak tests also showed no errors
However, Block Transfers are not working yet. Observe different errors on block reads and writes (NB we also have evidence that RIO may not be generating write bursts correctly.) But both effects in FED are reproducible. Diagnostics collected and design will be examined when Ed is back from leave.
NB In addition to firmware, these measurements also test new VME buffer chips & logic.

Next: Spend a couple more days on getting burst transfers going (NB burst is not essential yet.)
Then test serial engine data path (control/monitoring) from VME to BE FPGA (see below.)
Need this to be able to control settings at front end eg OptoRx control lines to aid OptoTests.

Back-End
Saeed has placed and routed fast data/address write to QDR. Still some uncertainties in timing. But tests of this logic can start in parallel (see below.)
VME-Link readout is also partially implemented.
FIFOs with APV frame header data done.

Next: Implement control logic for VME-Link reads (i.e. back pressure, fill flags.)
Include Emlyn's DAQ header block. Append Tracker header block.
Ed to include receiver end of serial path between VME and BE FPGAs.
Write test firmware for FE FPGAs to feed existing design for BE FPGA data path. Monitor inputs to QDR with ChipScope.

We have FED Kit from TriDAS, not looked at yet.
We also have DAQ PC from PPD in our lab, but not used yet.

FED-PMCs:
We may be able to assemble 10 PMCs a couple of weeks ahead of schedule.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Produce FED software driver lib API.		JC	29-11-02
Verify operation of first electrical test card.	Done	JS	
Run with Delay FPGA design in FED.		IC/EF	07-03-03
Test basic VME FPGA read/write interface.	Done	EF/MN/JC	
Deliver FED with 2 OptoRx to IC.		JC	28-03-03

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Produce FED software driver lib API.	JC	01-04-03
Run with Delay FPGA design in FED.	IC/EF	21-03-03
Debug block transfer VME FPGA.	EF	21-03-03
Get OptoTest card bench working at RAL.	MN	21-03-03
Deliver FED with 2 OptoRx to IC.	JC	28-03-03
Test serial comms between VME and BE FPGA.	EF/JC	28-03-03
Test FE to BE FPGA and QDR data write path.	IC/ST	04-04-03

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** J. Coughlan **Date:** Wednesday 19-March-2003		**PMF number: 27** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off &PCB Tape Out**	**07.10.02**		**06.12.02**
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**		**22.01.03**
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		