Project Monitor Form

Project: CMS FED **Date:** Wednesday 19-February-2003	**PMF number: 25** **Sheet:** 1 **of** 2

Project Implementation phase.

Status:

Testing is progressing well.

VME Extender card (with P0 connector) used to complete loop back Boundary Scan on ser 001. Test passed without errors.

Collection of minor mods learnt from experience with ser 001 were applied to ser 002.
Boundary Scan tests on ser 002 were completed successfully. After fixing few solder bridges on resistor packs (as done on ser 001)there were no errors.

Boundary Scan tests now completed.

No additional bugs found on ser 002 yet.

Route cards for both boards are being kept up to date.
Plus a list of general mods for next iterations.

Crate 3.3 V supply was increased on Power Supply to compensate for drop (200 mV?) on board.

Full chain of FPGAs et al (36 devices) successfully programmed using USB/Parallel cable and Xilinx tools.
NB Full loading via USB cable takes 2-3 mins. Loading from file via parallel cable takes 6 mins.
System ACE from CFlash?
VME FPGA is always now programmed at boot from EPROM (as intended in normal operation.) (NB Incorrect BSDL file for System ACE controller was preventing direct loading of VME FPGA previously reported.)

But a software problem with Xilinx tools prevents saving configuration file for more than 30 devices on a chain? Reported to Xilinx, but still awaiting fix.
Consequence of this is that re-loading procedure after power on is very tedious as each device in chain has to have an individual file explicitly assigned to it.

This bug also prevents testing SystemACE CFlash card loading (same software is used to create CFlash card files.)

If no fix comes from Xilinx in near future we could bypass some devices on JTAG chain (i.e. skip loading one FE module) to circumvent this software bug.

Basic test firmware distributes clock from Oscillator from backend FPGAs to ADCs via FE and Delay FPGAs.
Quick look at spread of clock phases between channels at FrontEnd looks reasonable 200-300 psec. But this needs more thorough measurement.

Currently trying to use ChipScope to capture ADC outputs.

We had a problem with installing ChipScope in test design. Eventually obtained a patch from Xilinx to make it work. (But ChipScope had been working earlier on the development board?) Also discovered that ChipScope tools do not work with USB cable!

Now updating test firmware to enable ADCs and to trigger and capture on appropriate signals.

Starting to observe pedestal levels captured in Delay FPGA. Still learning how to use graphic "bus" displays in ChipScope tools.

Next steps…

Measure analogue inputs to compare with observed pedestals.

Still need to verify that controls to ADCs are being driven in expected mode (gain etc). ADCs run hot until the FPGAs are programmed. This is not expected default behaviour which should put ADCs in power down mode.

Then can input signals using signal generator directly on single channel.
NB Electrical test card (for multiple channel tests) won't be available until start of week 10 (see below.)

Conclude:
Testing is still progressing according to original Test Plan schedule.
Earliest completion of (very) basic analogue tests at RAL on first board is end of week 10.

Board to IC:
Need to decide how to fit OptoRx (and how many) for IC tests.
And how to pass synchronous clock and trigger (frame synch) to FED from OptoTest card (or TTC system?)

Electrical Test Card:

Design sent out which relies on using original test connectors on FED mother board. Putting pins on test card was proving too complicated.
24 PCBs manufactured.
10 assembled cards (we have 10 cross point chips) should be delivered end of next week (#9).
Extra cards can go to IC.

Firmware:
Zipped versions of all FPGA firmware will be sent to Emlyn by end of this week. This will permit work to start on writing software models of the FED firmware for verifying board operation.
NB There is still a general FPGA tools problem with hardwired. library pathnames in designs.
It was accepted that these are not the final designs (in particular the BE and VME FPGAs are still very much work in progress.)

Agreement was made that the final bit streams for loading FPGAs will always be created at RAL. (i.e. firmware version management will be co-ordinated from RAL.)

FED-PMCs:
Requisitions in progress for 40 more PMCs (actually ordering 50 off for more critical components.)
Manufacture of 50 PCBs in progress (Express Circuits).

PMC test bench and equipment was moved to new FED area in Lab.

PMC nrs 47 & 49 returned from CERN module testers with Xilinx loading errors. Now under investigation.

For compatibility we recently obtained from CERN group an EP manufactured PMC carrier (as used in module test stations.)

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Produce FED software driver lib API.		JC	29-11-02
Organise lab space for FED tests.	Done	RH/JC	
Prepare loop back test for JTAG..	Done.	ST/RM	
Release updated designs for BE & VME Firmware	Awaiting library name fix	RH	24-01-03
Arrange for Matt Noy to work part time at RAL.	Done	JC	
Complete JTAG (loop back) tests on ser 001.	Done	ST/RM	
Load all FPGAs on JTAG chain using Xilinx cable.	Done	ST/EF	
Give go ahead for electrical test tape out.	Done	JS	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Produce FED software driver lib API.	JC	14-03-03
Release updated designs for BE & VME Firmware	RH	28-02-03
Capture sine wave output from ADCs on one FE module channel.	ST/EF	21-02-03
Verify operation of first electrical test card.	JS	28-02-03
Send zipped versions of current firmware to IC.	ST	21-02-03

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 25**		
Project Manager: J. Coughlan **Date:** Wednesday 19-February-2003		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off &PCB Tape Out**	**07.10.02**		**06.12.02**
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**		**22.01.03**
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		