Project Monitor Form

Project: CMS FED	**PMF number: 09**
Date: Monday 18-February-2002	**Sheet:** 1 **of** 2

News and comment
Feasibility Study continues.

Manufacture:
Bob has not yet had any replies to the request for quotes on AD8138 ARM.
We have been quoted reduction (by Impact Memec) of 25% on 3M parts for orders >100 (now £360). We will request comparable quotes on 1.5 and 2M parts.

In order to get an estimate of production FED manufacturing costs Chris has obtained a quote for 500 off H1 FTT, 20 day, of £70 (cf £ 230 for 8 off, 5 days.) Company **EXPRESS CIRCUITS**.
Based on these figures Adam extrapolates an estimate for 500 off FED of £150.
This can be considered together with previously obtained quote for assembly of 500 H1 FTTs at £300 (cf £700 30 off). Company **CEM GRAFT**.

Front End Module:
Chris is still working on the first order module layout. He is experiencing problems with the design tools (Allegro) whilst stripping components from modules.

James and Adam have reviewed schematic from Chris and annotated changes. So far only minor component value changes identified.
Chris will go ahead with layouts for original single channel ADC and OptoRx/VREF circuits and incorporate these changes later.
There has been no progress in automated importing of Xilinx devices into design library. If it has to be done manually estimate is a week / device.

Adam produced a list of recommendations for changes to the pinout of the OptoRx. This has been sent to CERN, but as yet there has been no reply.

In simulation James has identified 0.3% signal effect caused by VREF chain at frequencies of 3kHz. He will investigate circuit further using evaluation board.

He has also further studeied temperature/voltage monitoring devices. He has suggested improvements to the first scheme of monitoring VREF signal. New scheme would use one device for monitoring close to Opto Rx and another for a group of FPGAs. He will make a proposal for the next design meeting.

James is also continuing design of PS filters for supplies to OptoRx, VREF/ADC drivers and ADCs. Some proposed components are obsolete and need replacements.

Firmware:
Delay FPGA:
Ed (with a little help from Rob and Xilinx) has solved the problems in obtaining 360 degree independent phase control on all 4 DCM channels. He has tested repeatable scanning on 3 channels on the evaluation board (the 4th is probably ok too.) There is a slight jump at 180

degrees, but this can be compensated for.
He has put back the spy data and has verified the updated design with synthesis tools. He will investigate if it is possible to test it on the evaluation board. However, the board uses engineering samples of FPGA and has some restrictions on the i/o (and other features) which makes it difficult to implements Ed's full design.
He has also done a basic test of DCI. He can see the influence of enabling DCI although the scope/probes don't permit a detailed study of overshooting.
Ed intends to deliver a pinout for inspection by Adam by the end of Feb.
He will also look at clock input options (LVDS?) and external circuitry needed by FPGA

Front End FPGA:
Bill has re-synthesised his design in 3M part. It uses a little under 60 % of the resources of this device.
He is still having some problems using the tools with constraining clock signals.
It may be that it is already meeting timing requirements, but he just can't verify it.
Note: Synthesis turn around is an order of magnitude better with the new PC.

Back End FPGA:
Ported Azmat's design to John's laptop. Simulation running. Design needed couple of minor fixes for FPGAdv5.2. Next step is to integrate daq header block from Emlyn Corrin.

Board level:
Saeed has produced a first table of current requirements for analogue components and a draft power distribution block diagram.
He has also produced a draft block diagram for the JTAG chain.

Other issues:

Actions from the previous PMF

Action	Status	Who	Target date
Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	In progress	EF/RH	31-02-02
Produce pinout of Delay FPGA for inspection by Adam.	In progress	EF	11-02-02
Obtain estimate for PCB manufacture 500 H1FTT as guide of CMS costs.	Done	CD	
Produce recommendations for OptoRx pin out.	Done	AB	
Specify board level voltage and current requirements.	First draft produced.	ST	
Make request to R. Stephenson to borrow simulations tools license for James's PC.	On going	RH	11-02-02

Investigate temperature monitoring of FE Module (OptoRx/ Virtex)	Done	JS	
Produce proposal for web pages reorganisation	Done	AB	
Check Chris's schematic.	Done	JS/AB	
Produce 1st order FE module analogue component layout.	In progress	CD	25-02-02
Pass ADC driver component details for purchase this FY to Bob.	Done	JC	

Actions outstanding and new actions

Action	Who	Target Date
Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	EF	04-03-02
Produce pinout of Delay FPGA for inspection by Adam.	EF	04-03-02
Make request to R. Stephenson to borrow Orcad professional simulations tools license for James's PC.	RH	11-03-02
Produce 1st order FE module analogue component layout.	CD	25-02-02
Produce proposal scheme and devices for temperature monitoring of OptoRx and FPGAs.	JS	04-03-02
Find out from Paul Hardy whether it is possible, and if so how, to automatically generate Xilinx FPGA symbols in CADENCE.	RH	11-03-02
Request quotes from Impact for 1.5 and 2M FPGA parts.	RH	25-02-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 09**		
Project Manager: R. Halsall **Date:** Monday 18-February-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.0**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	**Project Spec sign off**	**21-12-01**		**05-02-02**
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	11-03-02	
5	FE Module Feasibility Review	28-02-02	11-03-02	
7	**Board Level Feasibility Review**	**04-03-02**	**08-04-02**	
8	Delay FPGA Interim Review	31-01-02	04-03-02	
9	Front End FPGA Interim Review	31-01-02	04-03-02	
10	Back End FPGA Interim Review	31-01-02	25-03-02	
11	VME FPGA Feasibility Review	28-02-02	25-03-02	
12	Clock FPGA Feasibility Review	28-02-02	25-03-02	
13	Release Test Plan Document	22-02-02	08-04-02	
14	FE Module Final Review	30-04-02		
15	BE Board Final Review	10-05-02		
16	Full Board Design Final Review	31-05-02		
17	**IDR Customer Production sign off**	**10-06-02**		
18	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**26-07-02**		
19	OptoRx for Batch 0 at RAL	26-08-02		
20	**Batch 0 Opto Assembled boards at RAL**	**01-11-02**		
21	Batch 0 review	06-01-03		
22	**Batch 1 (8 off) Assembled boards at RAL**	**21-03-03**		
23	**Delivery Batch 1 to CERN completed.**	**11-07-03**		