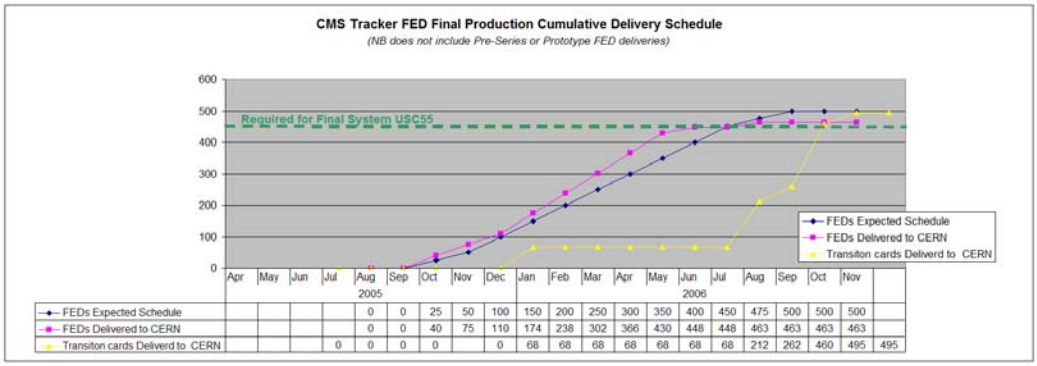
Project Monitor Form

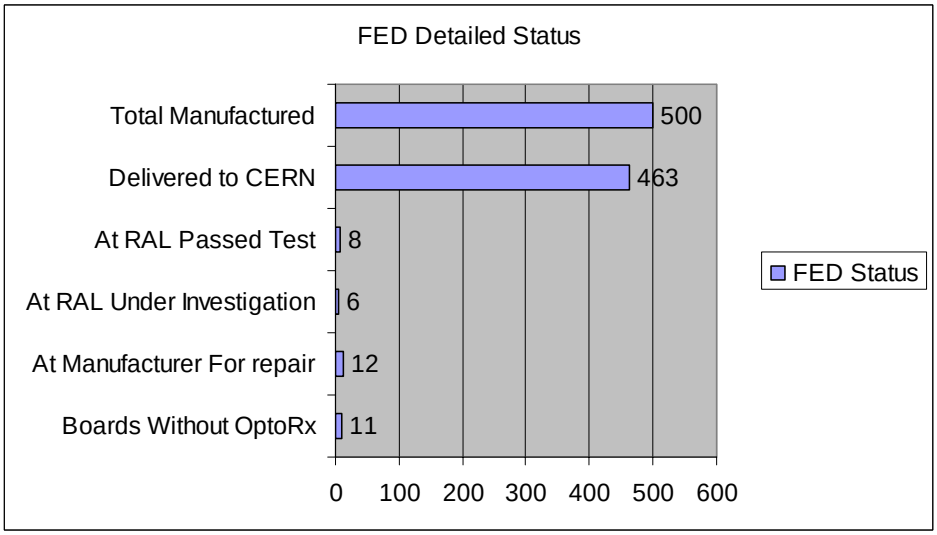
Project: CMS FED **Date:** Friday 11 November-2006	**PMF number: 64** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production



	Apr	May	Jun	Jul	Aug 2005	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun 2006	Jul	Aug	Sep	Oct	Nov	
FEDs Expected Schedule					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500	
FEDs Delivered to CERN					0	0	40	75	110	174	238	302	366	430	448	448	463	463	463	463	
Transiton cards Deliverd to CERN				0	0	0	0		0	68	68	68	68	68	68	68	212	262	460	495	495



Full details in Production spreadsheet.

FEDs

An end of FED Production Review meeting was held at Exception on 5th October.
We located the “missing” FED (R079) which turned out to be marked as scrap due to BE FPGA assembly and power section failures.
All other (spare) boards are accounted for. A couple were ready to go back to RAL. Several are awaiting FPGA rework. And a few are being “unwarped”.

If up to (5?) boards cannot be repaired we will recover their ORx and move to unpopulated boards.
In the unlikely event of 5 or more boards we will need to consider another Fast Track run.
Nb There are no spare PCBs.

No more shipments since last report i.e. still 463 at CERN.

Another 8 more boards are ready if needed. But prefer to wait until we have a crateful ~ 16 before shipping more.
Ivan is continuing to investigate another 6 in hand (in parallel with work at CERN). By their nature they may have more subtle problems to understand.
We are also waiting for several boards from Exception to have one FPGA each replaced (see above). But this appears delayed due to lead times for spares. It's difficult to give an estimate for delivery of remainder until we have retested these boards.
But it is likely that we will still have a dozen or so boards (with ORx) undelivered at the end of 2006.

We propose to hold the 11 boards without OptoRx at RAL pending further ORx deiliveries (see mail below).

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Dear Geoff, John,

I looked into the possibility of supplying additional NGK modules:
- NGK sees a possibility to manufacture 70 to 80 modules with the pieceparts
remaining at their factory.
- The 2-year guarantee on the last pieces supplied in 2005 will expire in Sep
2007.
- We could supply ~20pcs from our QA-reference stock, assuming no problem is
reported during FED testing/commissioning.

This would allow you to populate up to 8 FEDs at the end of 2007.

Are these timescales reasonable?  Would there be money to purchase the
contingency modules from NGK at a possibly higher price than during
production?

Cheers,
Francois
```

SLINK Transition Cards

SLINK testing was completed in October. A handful of cards that gave errors earlier were repaired. All 500 have now passed tests. i.e. Yield = 100%.
495 are now at CERN. 5 have been kept at RAL.

CERN USC Installation and Commissioning :

Ivan assisted with installing first couple of crates in USC.
He also spent another week working in TIF (186) learning installation procedures and testing fibres to the Tracker.

Final crates arrived in November (see notes from Oz below).

```
Our 22 crates have arrived. I have picked and installed 4 in 904 and the
remaining will be delivered to 904 sometime next week.

Secondly, the VME controller fibres of the 3 Tracker crates in USC55 as well
as the PCI and VME controllers are ready. We now need to install the turbines
and connect the VME controller fibres on the PC end as well as install the
necessary software to test the rack.

As for the installation of the crates in USC55, it will have to wait
(probably until Jan. 07) since  S1 in USC55 is not ready for installing the
crates - pipes everywhere, de-humidifier is not working, etc.
```

System Integration Tests

Problem with latest firmware in CERN FRL test system under intensive investigation….

1. The slink readout in 904 using an older version is ok.
2. The slink readout in 904 using FE_33C.bit and BE_7D.bit are ok.
3. SLINK readout in 904 using FE_33D.bit and BE_7E.bit (latest firmware) does not work correctly.
    3a) the L1A counters are counting but no events are received through slink txr/rxr cards.
    3b) JF has tried VLINK read out and it is ok. This indicates the format of the events are correct and they exist!
4. SLINK readout in RAL using FE_33D.bit and BE_7E.bit (latest firmware) does work correctly
5. VLINK readout in 904 using FE_33D.bit and BE_7E.bit (latest firmware) does work correctly

The fact the firmware does work at RAL and partially works at 904, makes finding the problem even harder.

Firmware :

List of proposed changes according to Saeed

```
1. Swap FE Full Flag with FE Partial Full Flag. This is the mod I have done
and sent you the ACE file (10_11_06) . Unless this is tested and found to be
ok, I will not be able to implement the rest of the mods.

2. Add 8 FE Full Flags to the register in the Special Tracker Header. This
register would indicate that any one FE FPGA buffer has entered the overflow
condition. This needs to be investigated in order to find out how best to use
it to indicate the payload data is corrupt/overwritten. I will try to discuss
with Oz re best way to implement.

3. Change BE Status Register Two from 64 bits to 32 bits (already discussed
with JF and Jo).

4. Does JF require a reset sent to the ACE System after a vme reset is
issued? At the moment this is not happening. Need to discuss with JF. This is
to do with problems reading DLY FPGA after an ACE file upload.

5. Remove TTC_Ready signal from the BE Command Decoder, as this is redundant.

6. Store the two software DAQ registers in the Tracker Headers in a FIFO at
the time L1A is received (requested by JF).
This is the most complex mod at this stage of development. Therefore all
other mods must be checked to ensure no errors are introduced in the BE f/w
before this change is made.
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Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Complete delivery of 450 Transition cards to CERN.	Done. All 500 tested and 495 delivered.	IC	
Test BLT for System ACE CF loading		JC	01-11-06
Fix Synchronisation problems seen in MTCC	Needs error to be reproduced at CERN.	ST	01-11-06
Decide on event format proposal.		JC	01-11-06

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Test BLT for System ACE CF loading	JC	01-04-07
Fix Synchronisation problems seen in MTCC	ST	01-04-07
Decide on event format proposal.	JC	01-02-07
Understand and fix problem with FRL readout.	ST	01-12-06
Implement DAQ header registers in FIFOs.	ST	31-12-06

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 64**		
Project Manager: J. Coughlan **Date:** Friday 11 November-2006		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05		28.07.05
33	Production of 500 FEDv3 starts	08.09.05		01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05		27.10.05
35	First FED installed at USC55	17.11.05		19.10.06
36	Last FED installed at USC55	26.07.06	01.06.07	
37	Power on Tracker at USC55	01.08.06	01.07.07	
38	Readout test with Tracker at USC55	01.10.06	01.08.07	
39	LHC test run	02.04.07	01.11.07	