

Project Monitor Form

Project: CMS FED

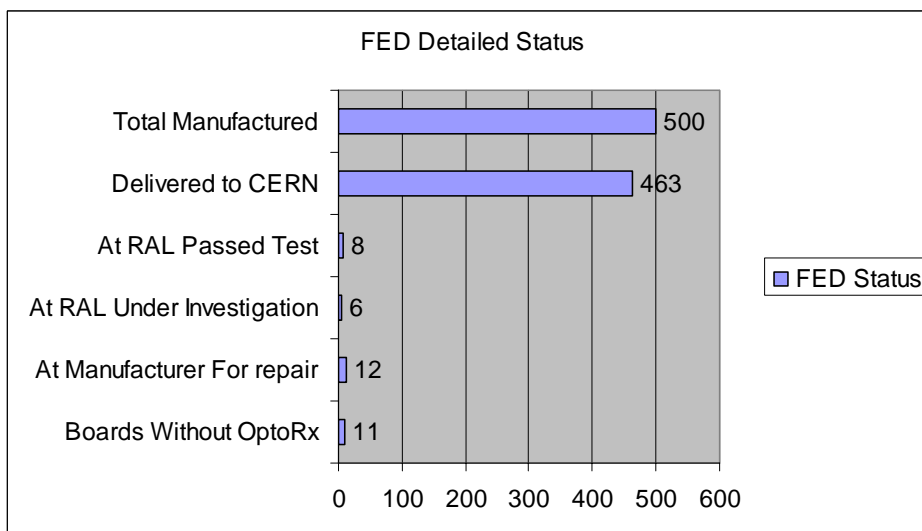
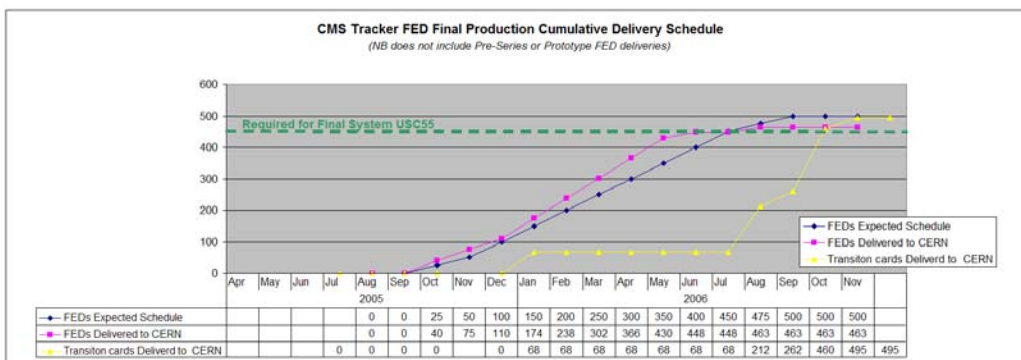
Date: Friday 11 November-2006

PMF number: 64

Sheet: 1 of 2

Project Implementation phase.

FED Production


 Full details in Production [spreadsheet](#).

FEDs

 An end of FED Production Review meeting was held at Exception on 5th October.

We located the "missing" FED (R079) which turned out to be marked as scrap due to BE FPGA assembly and power section failures.

All other (spare) boards are accounted for. A couple were ready to go back to RAL. Several are awaiting FPGA rework. And a few are being "unwarped".

If up to (5?) boards cannot be repaired we will recover their ORx and move to unpopulated boards.

In the unlikely event of 5 or more boards we will need to consider another Fast Track run.

Nb There are no spare PCBs.

No more shipments since last report i.e. still 463 at CERN.

Another 8 more boards are ready if needed. But prefer to wait until we have a crateful ~ 16 before shipping more.

Ivan is continuing to investigate another 6 in hand (in parallel with work at CERN). By their nature they may have more subtle problems to understand.

We are also waiting for several boards from Exception to have one FPGA each replaced (see above). But this appears delayed due to lead times for spares. It's difficult to give an estimate for delivery of remainder until we have retested these boards.

But it is likely that we will still have a dozen or so boards (with ORx) undelivered at the end of 2006.

We propose to hold the 11 boards without OptoRx at RAL pending further ORx deliveries (see mail below).

Dear Geoff, John,

I looked into the possibility of supplying additional NGK modules:

- NGK sees a possibility to manufacture 70 to 80 modules with the pieceparts remaining at their factory.
- The 2-year guarantee on the last pieces supplied in 2005 will expire in Sep 2007.
- We could supply ~20pcs from our QA-reference stock, assuming no problem is reported during FED testing/commissioning.

This would allow you to populate up to 8 FEDs at the end of 2007.

Are these timescales reasonable? Would there be money to purchase the contingency modules from NGK at a possibly higher price than during production?

Cheers,
Francois

SLINK Transition Cards

SLINK testing was completed in October. A handful of cards that gave errors earlier were repaired. All 500 have now passed tests. i.e. Yield = 100%.

495 are now at CERN. 5 have been kept at RAL.

CERN USC Installation and Commissioning :

Ivan assisted with installing first couple of crates in USC.

He also spent another week working in TIF (186) learning installation procedures and testing fibres to the Tracker.

Final crates arrived in November (see notes from Oz below).

Our 22 crates have arrived. I have picked and installed 4 in 904 and the remaining will be delivered to 904 sometime next week.

Secondly, the VME controller fibres of the 3 Tracker crates in USC55 as well as the PCI and VME controllers are ready. We now need to install the turbines and connect the VME controller fibres on the PC end as well as install the necessary software to test the rack.

As for the installation of the crates in USC55, it will have to wait (probably until Jan. 07) since S1 in USC55 is not ready for installing the crates - pipes everywhere, de-humidifier is not working, etc.

System Integration Tests

Problem with latest firmware in CERN FRL test system under intensive investigation....

1. The slink readout in 904 using an older version is ok.
2. The slink readout in 904 using FE_33C.bit and BE_7D.bit are ok.
3. SLINK readout in 904 using FE_33D.bit and BE_7E.bit (latest firmware) does not work correctly.
 - 3a) the L1A counters are counting but no events are received through slink txr/rxr cards.
 - 3b) JF has tried VLINK read out and it is ok. This indicates the format of the events are correct and they exist!
4. SLINK readout in RAL using FE_33D.bit and BE_7E.bit (latest firmware) does work correctly
5. VLINK readout in 904 using FE_33D.bit and BE_7E.bit (latest firmware) does work correctly

The fact the firmware does work at RAL and partially works at 904, makes finding the problem even harder.

Firmware :

List of proposed changes according to Saeed

1. Swap FE Full Flag with FE Partial Full Flag. This is the mod I have done and sent you the ACE file (10_11_06) . Unless this is tested and found to be ok, I will not be able to implement the rest of the mods.
2. Add 8 FE Full Flags to the register in the Special Tracker Header. This register would indicate that any one FE FPGA buffer has entered the overflow condition. This needs to be investigated in order to find out how best to use it to indicate the payload data is corrupt/overwritten. I will try to discuss with Oz re best way to implement.
3. Change BE Status Register Two from 64 bits to 32 bits (already discussed with JF and Jo).
4. Does JF require a reset sent to the ACE System after a vme reset is issued? At the moment this is not happening. Need to discuss with JF. This is to do with problems reading DLY FPGA after an ACE file upload.
5. Remove TTC_Ready signal from the BE Command Decoder, as this is redundant.
6. Store the two software DAQ registers in the Tracker Headers in a FIFO at the time L1A is received (requested by JF).
This is the most complex mod at this stage of development. Therefore all other mods must be checked to ensure no errors are introduced in the BE f/w before this change is made.