Project Monitor Form

Project: CMS FED **Date:** Thursday 17-October-2002	**PMF number: 19** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

Personel:
Due to additional management responsibilities within the department Rob has stepped down as Project manager. John Coughlan has taken over the role effective 20.09.02. Rob remains on the project as the Technical manager. The customer has agreed to the change.

Staff Effort:
Staff effort **FY 2002/2003** April-September = **2.7 SY** (c.f. **3.1 SY** projected)
Project effort in next 6 months is expected to be ~ 2.5 – 3 SY.
Customer has not requested any special actions to be taken.

Procurement:
Customer has asked us to prepare procurement for a further 20 FF1 boards for manufacture in Q3 2003. He would also like to increase our spend in this FY.
As FPGAs may be on longer lead times we have started by asking for quotes on these.
Estimated spend on FPGAs (based on previous estimates) for 20 boards would be £50 K.

Manufacture:
Assembly company choice is between CemGraft and SAE Tech.
The former did the H1 FTT ADC boards. The latter did the Generic ADC cards.
There have been some quality problems recently reported on the recent batch of 30 boards (related to BGAs and TQFPs).
NOTE: Customer has recently expressed concern about quality of BGA assembly on some CERN projects.
Layouts have been passed to SAE Tech for feedback and quotes.

Schedule:

A meeting was held to find a solution to the problems of the migration of Cadence layout tools from 13.x to 14.2 (attended by Steve Quinton, Paul Hartley, Chris Day, Rob Halsall and John Coughlan).

There was a fundamental problem with the Database containing the converted design which preventing any progress with design work. Cadence were contacted and they subsequently suggested a solution which worked. It turned out that all the steps necessary for the conversion process hadn't been completed even though the messages from the conversion program appeared to indicate that it had.
A second basic problem arose in the following week. This prevented modules being created. A further correspondence with Cadence resulted in obtaining some more documentation which explained how to achieve correct module creation.
It should be noted that neither problem was specific to the FED design.

Several factors have contributed to this situation. Although Europractice have been very helpful in resolving this situation, a major difficulty is the inability of the drawing office to contact Cadence directly or to access Cadence release notes etc. The need to convert through several releases of the tools at once also did not help the situation. Neither did the fact that only one member of the drawing office was permitted at first to use the new version. The online documentation does not seem to be adequate. The drawing room staff have also not received formal training with these new tools.

Migrating a test design ahead of schedule would have unearthed these problems.

In total about 3 weeks of layout and routing work were lost due to the tools migration difficulties. The customer has expressed his deep unhappiness at this situation.

However, the advantages of using **v 14.2** cf 13.x for modular design have now been demonstrated. The speed of layout has increased considerably and more reliable netlists can now be produced.
With the new tools installed the layout and routing work is again progressing well (see below). The critical path of the schedule remains in Drawing office.

We are now aiming to go out for manufacture in **week 46** (starting November 11th).

Design:
For details refer to minutes of FED Design Meeting 16th October.

Chris did a preliminary layout of the whole board based on Rob's baseline. The various sections were then accurately positioned after discussions with Saeed, Rob and James. There were no major difficulties encountered.
Chris is now completing the routing within the Front-End Module. Once this is done (early next week) the routed FE modules will be brought back in to board level.
Some final adjustments to the back end layout have already been identified. In particular, the BE FPGA will be placed as close as possible to P2 to ensure the integrity of the fast DAQ link signals.
After board level routing is done the Power/Gnd planes will be implemented.
Chris then estimates one week to prepare drawings etc before going out to manufacture.

Saeed considered changing clock feedback mechanism to external feedback as expected in Azmat's BE FPGA design. After discussing with Rob it was decided not to do this as it would entail a lot of changes to the pinouts and might not bring much benefit. Internal feedback should be adequate.

Test:
For details refer to minutes of FED Design Meeting 16th October.

Electronics division management are keen for RAL to fully qualify the FED electrically.
James has been appointed manager of FED test activities at RAL.

Firmware:
For details refer to minutes of FED Design Meeting 16th October.

VME FPGA: Ed has now implemented 32 bit Block Transfers and tested with back annotated

timing model.
BE FPGA: Saeed has started implementing Rob's improved QDR address generation scheme.

Software:
Basic memory map has been proposed. Needs further discussion on implications for firmware design.
Software specification is now a critical path item for CMS module testers.

Crates:

John and Rob drew up a requirements list for the FED crates.
This has been distributed to IC for comment before going to CERN.
Rob has identified a PSU for test system.
Costas Foudas (IC) has identified a VME64x backplane.

Matthew Pearson (PPD) has produced a proposal for arranging FEDs in crates.
In this scheme the maximum number of FEDs/crate would be 16.

DAQ:
TTS signal definitions have changed. All 4 lines are now encoded. Doesn't affect layout.

IC now have a FED Kit (for S-LINK testing.) This requires a special PC with dedicated 64bit/66MHz PCI bus. RAL will get a FED Kit in Q1/2003.
Matt Noy (IC) has got basic XDAQ software working. He has also been able to talk to VME crate using provided NI/VXI drivers.
We need to clone the IC system at RAL.

DAQ group are interested in common solution for CRC. Emlyn Corrin (IC) has already implemented one.

Actions from the previous PMF

Action	Status	Who	Target date
Review VME firmware.	Done	JC	19-09-02
Produce FED memory map.	Draft proposal done.	JC	16-10-02
Produce FED software driver lib API.	Done	JC	29-11-02

Actions outstanding and new actions

Action	Who	Target Date
Complete FE module routing.	CD	22-10-02
Final adjustments to Board level layout complete & reviewed.	CD	24-10-02
Schematics and netlist released.	CD	25-10-02
Board level routing completed.	CD	08-11-02
FED sign off and out to manufacture.	JC/EF	15-11-02
Review FED memory map..	JC	22-10-02

Produce FED software driver lib API.	JC	29-11-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 19**		
Project Manager: J. Coughlan **Date:** Thursday 17-October-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02	31.07.02	12.08.02
10	Back End FPGA Interim Review	04.03.02	30.08.02	
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02	26.07.02	15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02	08.11.02	
15	Full Board Design Final Review	23.09.02	11.11.02	
16	**IDR Customer Production sign off**	**07.10.02**	**14.11.02**	
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**	**06.12.02**	
18	OptoRx for Batch 0 at RAL	26.08.02		
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.02		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		