Project Monitor Form

Project: CMS FED **Date:** Monday 16-September-2002	**PMF number: 18** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

Schedule:
Critical path of work is now in Drawing office.
Schedule has slipped by approximately 2 weeks (with respect to **v 1.3).** Principle reason is inability of layout and routing tools to handle the modular PCB design (see below).
The situation has to be reviewed at the end of this week 38. A decision must then be made whether to persevere with Cadence v14.2 (in the hope that it will eventually work and speed up our progress) or go back to v13.6 (with all the previous hangups which were slowing down layout and routing).

Best we can expect now is for assembled boards back at RAL by end of November.

Design:

Chris produced a board level netlist and schematics **v 22.08.02** for review. These incorporated all the design changes up to that date (using Cadence tools v13.6).
The netlists produced these tools did show up a couple of errors, but in general the lists proved difficult to check owing to the scrambling of the (modular) signal names by tools.
Rob attempted to analyse netlists with some Perl scripts.
The schematics were however checked again very carefully. A couple of minor bugs turned up and were corrected.

Some minor changes were subsequently made to the design. The associated change list has been updated.
Most important alteration was removal of recently added hot swap controller (on 1.5V).

➔ The design is now **FROZEN**.
(only changes required to fix errors and unavailable components will be accepted).

Saeed is studying in detail the layout options around BE FPGA and QDRs.

Lists of layout and assembly instructions have been produced.

Board level layout recommenced in week 34. Accumulated changes in FE modules were implemented. All routing within and between 3 sub-modules except for that between ADC and FE-FPGA modules were done. FE module was flattened.
In parallel, a flattened version of the schematics and associated netlist were also produced (see above).
Chris experienced a number of problems with Cadence tools v13.6 whilst doing this work. In particular, there were difficulties in moving within the hierarchy of the modular design and producing netlists.
In week 37 Chris obtained the latest Cadence tools v14.2 which has features optimised for

modular design.
The FED schematics were imported into the new tools. Initially results were encouraging. The new modular functionality aided design and speeded up the flow. Subsequently, however, there have been other problems with the new tools (whilst importing symbols on back end of board into the design.) The errors reported are proving difficult to interpret and the access to support and help information is rather indirect. Problems may be related to jumping design from v13.6 to v14.2.

As a consequence the layout of the back-end of the board has not been started as was anticipated.

Test:

A draft Test Plan v0.1 was presented at the customer meeting on Sept 3rd.
IC are keen to obtain a FED as soon as possible after basic tests are carried out.
In this scheme IC would take over the optical and advanced analogue testing on one board whilst RAL is testing the digital design on the other.

Firmware:

Ed Freeman has implemented a very simple VME FPGA interface (based on Rob's suggestions). It is imperative now to obtain a memory map and prepare programming model of FED (see below).

At customer meeting on Sept 3rd Rob presented a scheme to obviate need for transition card for DAQ link. This moves the channel link LVDS design now on DAQ link PMC into our BE-FPGA (Xilinx provide application notes explaining how to do this). The DAQ link signals would come directly out of J2 connector with plug on cable.
The current BE-FPGA pin-out is compatible with both solutions.
The DAQ link cables would need to be modified at our ends to take the J2 connector.

Customer is very interested to adopt this solution owing to the savings involved.

DAQ issues:

Discussion with CERN LHC crates responsible. DAQ link transition card (if required) should be 6U (220mm deep) and located at bottom of crate. Standard PS would be located above (behind P1).

Rob's scheme for avoiding transition card for DAQ link was raised with CERN DAQ responsible. DAQ commented that scheme may not work if links design is modified.

Customer has asked us to produce a list of our crate and PS requirements by end of September. Ordering of first batches of LHC standard crate will begin by the end of the year.

Tracker groups have requested schedule for delivery of programming models and/or software drivers for FED in order that they can prepare software for silicon module tests.

AOB:

FED paper was presented at LHC Electronics Workshop, Colmar France, Sept 9-13th.
Next customer meeting at RAL Sept 19th.

Actions from the previous PMF

Action	Status	Who	Target date
Implement final FE & BE schematic changes prior to layout.	Done (design frozen)	ST	
Flatten copy of schematics at board level. Distribute electronic version.	Done	CD	
Release board level netlist.	Done	CD	
Review board level netlist.	Done	ST/JC	
Release board level Bill of Materials.	Done	CD	
Complete FE module layout.	All except ADC to FE-FPGA module done.	CD	
Release first version of board level layout.	Done	CD	06-09-02
Produce draft test plan.	Done	JC	

Actions outstanding and new actions

Action	Who	Target Date
Complete FE-FPGA module layout.	CD	11-10-02
Release first version of board level layout.	CD	04-10-02
Review VME firmware.	JC	27-09-02
Produce FED memory map.	JC/EF	31-10-02
Produce FED software driver lib API.	JC	29-11-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 18**		
Project Manager: R. Halsall **Date:** Monday 16-September-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	**Project Spec sign off**	**21-12-01**		**05-02-02**
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02		21-03-02
5	FE Module Feasibility Review	28-02-02		08-05-02
7	**Board Level Feasibility Review**	**25-02-02**		**25-02-02**
8	Delay FPGA Interim Review	11-03-02		27-03-02
9	Front End FPGA Interim Review	28-02-02	31-07-02	
10	Back End FPGA Interim Review	04-03-02	30-08-02	
11	FE Module Final Review	18-06-02		25.06.02
12	BE Module Interim Review	28-06-02	26.07.02	15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02	11.10.02	
15	Full Board Design Final Review	23-09-02	18-10-02	
16	**IDR Customer Production sign off**	**07-10-02**	**25.10.02**	
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11-11-02**	**29.11.02**	
18	OptoRx for Batch 0 at RAL	26-08-02		
19	Batch 0 review	11-04-03		
20	OptoRx for Batch 1 at RAL	01.04.02		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04-07-03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04-12-03**		