Project Monitor Form

Project: CMS FED **Date:** Friday 16-August-2002	**PMF number: 17** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

Schedule:

We have kept to week by week work schedule (dated 25.07.02 and consistent with Project schedule **v1.3**).
FE and BE schematics were reviewed on **15.08.02**.
Final updated schematics will be produced by Saeed (with lists of inter-module i/o and changes implemented together with any special instructions) for Chris to start board level layout on his return from leave on 19.08.02.

Expenditure:

Costings updated **v2.6**
FF1 prototype estimate **20.5 KCHF** ; FF3 production estimate **9.5 KCHF**
(both compatible with previous estimates.)
Largest uncertainties are still on PCB manufacturing and assembly costs.

Staff Effort:

Staff effort in **FY 2001/2002** was **4.9 SY** (c.f. **5.6 SY** projected.)
Small shortfall was expected due to delay in releasing design effort to project.
Customer has arranged to carry over unused effort to FY 2002/2003.

Staff effort **FY 2002/2003** April-June = **1.2 SY** (c.f. **1.5 SY** projected)
Staff effort usage to be reviewed every 3 months.

Design:

For details of design implementation and progress refer to minutes of FED design meetings of **August 15th**.

Carried out final review of schematics **version of 09.08.02** (prior to board level layout).
Resultant changes to be implemented by 19.08.02

List of significant design updates since PMF #15:

Front End Module:

CERN have confirmed design changes for OptoRx settling time (peaking caps, extra controls.)
OptoRx controls buffer chip changed.

BE Module :

TTC PIN diode differential True Light component fitted (option for single-ended maintained.)
TTS now brought to J0 (VME64x spec.) This allows connector option on J2 for S-LINK.

VME signals provided for VME 64x : A32/D64 Slave ; Geographic addressing ; with Interrupter ; Master (for DMA) Nb No slot1/arbiter functionality.
Hot swap compatible buffers employed. Pre-charge pins used.
Opto-couplers added to protect LM82 devices.

Preliminary (paper) layout of BE components done.
As a result, an additional (third) Hot Swap controller was introduced to simplify power distribution.

Firmware:

Bill Gannon's latest period of work completed:
Following implemented….
Double data rate I/O. Removed autocal. Simplified header checking. Added serial controls, bits n pieces Fits in 1500 device (75% full.) (using final pin constraints) Timing satisfied at 40 Mhz and 80 MHz in -4 part.
Nb Power calculation was not re-done.

Ed Freeman has recently rejoined to work on VME FPGA design.
Saeed Taghavirad will take over completion of BE FPGA design.

Testing:

Customer has requested preliminary test plan to be presented at next customer meeting.
Opto test board with 4 channels expected at ICL in September.

DAQ issues:

Document justifying use of VME64x crate as opposed to cPCI produced on request from customer.

AOB:

Next customer meeting at RAL Sept 3rd.
FED paper accepted for oral presentation at LHC Electronics Conf 2002 Colmar Sept 9-13th.

Actions from the previous PMF

Action	Status	Who	Target date
Pin out BE and VME FPGA blocks.	Done	ST	
Implement FE module final changes.	Done	ST	
Produce BE and VME FPGA block schematics rats nest.	Done	ST	

Produce BE and VME FPGA block schematics rats nest.	Done	ST	
Produce BE module layout (on paper.)	Preliminary done.	RH	
Incorporate latest modifications to FE FPGA firmware.	Done (all major changes)	WG	
Verify size, speed and power of FE-FPGA design.	Done (except for power)	WG	
Hold review BE module.	Done	JC	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Implement final FE & BE schematic changes prior to layout.	ST	19-08-02
Flatten copy of schematics at board level. Distribute electronic version..	CD	20-08-02
Release board level netlist.	CD	21-08-02
Review board level netlist.	ST/JC	23-08-02
Release board level Bill of Materials.	CD	23-08-02
Complete FE module layout.	CD	30-08-02
Release first version of board level layout.	CD	06-09-02

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** R. Halsall **Date:** Friday 16-August-2002		**PMF number: 17** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	**Project Spec sign off**	**21-12-01**		**05-02-02**
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02		21-03-02
5	FE Module Feasibility Review	28-02-02		08-05-02
7	**Board Level Feasibility Review**	**25-02-02**		**25-02-02**
8	Delay FPGA Interim Review	11-03-02		27-03-02
9	Front End FPGA Interim Review	28-02-02	31-07-02	
10	Back End FPGA Interim Review	04-03-02	30-08-02	
11	FE Module Final Review	18-06-02		25.06.02
12	BE Module Interim Review	28-06-02	26.07.02	
13	Schematics finalised	05.08.02		
14	Layout & Routing done	16.09.02		
15	Full Board Design Final Review	23-09-02		
16	**IDR Customer Production sign off**	**07-10-02**		
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11-11-02**		
18	OptoRx for Batch 0 at RAL	26-08-02		
19	Batch 0 review	11-04-03		
20	OptoRx for Batch 1 at RAL	01.04.02		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04-07-03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04-12-03**		