Project Monitor Form

Project: CMS FED	**PMF number: 30**
Date: Thursday 15-May-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

40 assembled PMCs now at RAL.
External clock and trigger tests setup.
First 5 PMCs fully tested and ready for delivery.
Just waiting for corrected Front Panels (stencils for lettering were wrong on first batch) expected this week.
Unfortunately we have a major upset with testing.
Test Engineer J. Godwin has just been called up (TA reserve.) He will leave in 2 weeks. He will be 100% testing PMCs till then. Try to get as many PMCs as possible.
Negotiating for a replacement. Need training period next week.

FEDv1:

Manufacture

Plan to assemble a further 3 PCBs.
Same components as 001/2 (except for footprint corrections) and..
But use XC2V1500's for FE-FPGAs (may need "FE-Lite" firmware, see below.) on all 3 boards.
Assemble one of boards with 8 OptoRx. After electrical testing at RAL exchange this with 001 at Imperial. Other 2 assembled without OptoRx's.
Reserve second board for dedicated tests of power circuitry. James has some ideas for improvements to ensure power circuit is stable when using all 8 OptoRx.
Send PCBs out next week. Allow further 2 weeks for assembly. Expect back end week 23.

Firmware

FE-FPGA:
Testing final design.
We can now send serial commands from VME to set up (some) registers in FE-FPGA.
We have tested OptoRx ctrls and Scope Mode set-up using basic software program (see below.)
Started to capture (on 1 FE module) data output in Scope Mode with s/w triggers. Partly working. See expected sequencing and correct total data length, but data contents are incomplete.
We also observe problems with ChipScope in FE-FPGA, whereby monitoring many (>50?) signals at once caused logic to misbehave. Lost us some time. We haven't seen these effects with other designs.
We have requested Bill G's assistance with debugging.

Also re-measured resource usage of FE FPGA design.

	XC2V2000	XC2V1500
Logic Slices	70%	95%
Block RAM	40%	50%

These numbers may appear worse than it is. No optimisations tried.

But had expected only 75% logic occupancy in 1500.
Therefore if some leeway is needed we may have to have a second “FED-Lite” design (e.g. without Clustering logic) for CERN boards.
But we still have spare Block RAMs. Suggest we try and increase depth of FIFO output buffers by concatenating Block RAMs. This would allow us to store more raw events in FE (back up to 6 or 7?)

BE FPGA:
Added logic to permit running in Scope mode with FE-FPGAs. But full timing simulations of QDR I/O are still failing (losing data packets.) Designer was on leave last week and is in hospital this week. Expect to resume tests sometime next week. Therefore have not loaded on FED yet. Meanwhile we continue to use test firmware in BE to exercise FE’s logic.

VME FPGA:
Testing read-back of FE registers.

Software
Hacked version of Matt’s FED Debug program used to exercise setting registers in FE-FPGA. Ready to test read-back path when implemented.
Matthew is working on a more elegant final implementation.