

Project Monitor Form

Project: CMS FED Date: Wednesday 15-January-2003	PMF number: 23 Sheet: 1 of 2
<p>Project Implementation phase.</p> <p><i>Status:</i> Waiting for first assembled FEDv1s to come back to RAL.</p> <p>2 FED PCBs arrived at RAL on 16th December. Checked and ok. (Remaining 4 FED PCBs arrived on 14th January as expected.)</p> <p>PCBs to Assembly company on 17th Dec.</p> <p>Assembly drawings were completed on 17th December.</p> <p>Replacement (of engineering sample) FPGAs XC2V40C arrived on 19th December.</p> <p>All necessary kit with Assembly company on 19th December.</p> <p>Had expected assembled boards by 10th January, but delays owing to bad weather. Assembly is in progress. Boards expected by 17th January. No problems with kitting or files reported from Assembly company.</p> <p>Front panel has been designed and is out for manufacture.</p> <p>Final FEDv1 schematic/layout files are on the web.</p> <p><i>Testing:</i> VME64x backplane was delivered from IC on 13th December. 9U crate has been assembled at RAL.</p> <p>Boundary scan tests are prepared except for loop back. Still awaiting VME64x Extender cards which will be needed for Boundary Scan loop back tests. We will need to build something if we don't receive them by today.</p> <p>Some simple test firmware has also been prepared (see below).</p> <p>Test bench area in Heavy Duty Lab has been cleared for FED work. Need to get another PC to run ChipScope etc (recycled from Rob.) Existing APV crate used in PMC tests has been moved there. But FED-PMC production bench will not be moved.</p> <p><u>Electrical Test Card:</u> Cross-point switch based electrical test card design was successfully reviewed and has been passed to Drawing office. The cross-point switch development board plus software has been tested and works as advertised.</p>	

All FED team members at RAL have attended basic laser safety course. Saeed Taghvirad has been nominated as Laser Responsible Officer and will attend advanced course this month.

RAL PPD have received same model PC as Imperial for DAQ S-LINK card tests. They also have loan of NI/MXI extender cards for Laser Driver Temp VME control tests.

Firmware:

Review of Backend FPGA designs was held on 19th December.

Rob proposed a nice scheme which would allow identical event data to be directed to either S-LINK or VME paths.

Concentrated logic on raw data readout over VME.

Redistributed logic between Back-End and VME FPGAs to exploit resources more efficiently. Need to get Emlyn involved. Update DAQ header format.

Some simple test firmware (for each FPGA on board) has been implemented.

It will distribute local oscillator clock around the board and flash some LEDs to verify FPGA download via JTAG is functioning.

Basic tests using Chip-Scope Core Logic Analyser in test design have been carried out.

Effort:

Tracker effort to date (up to and incl Dec) = 4.2 SY

Forecast 02/03 = 5.4 SY

CMS News:

Tested OptoRx are now ready to ship from CERN to RAL.

FED-PMCs:

PMC nrs 31 (fitted with EPROM) and 32 (ser nr reloaded) are ready for return to CERN.

Investigated procurement of a further production of FED-PMCs.

With no design changes.

All production and testing to be done at RAL.

Xilinx XC4036XL are being phased out by Xilinx. Last chance to buy.

Other parts seem ok so far.

New quote for PCB manufacture obtained. Assembly would be with SAETech. Test engineer effort reserved.

Ready to start production of another 20 off when given go ahead.

Estimate that PMCs would be ready for delivery by end of June if given go ahead now.

Next Meetings:

Tracker Week Electronics Mtg Wed 29th Jan

Actions from the previous PMF			
Action	Status	Who	Original Target date
Produce FED software driver lib API.		JC	29-11-02
Complete Assembly drawings.	Done	CD	17-12-02
Get FED Kit ready for Assembly company.	Done	BT	19-12-02
Store copies of FED schematics, drawings etc on project web.	Done	JC	19-12-02
Assemble VME crate.	Done	IC	16-12-02
Hold Back-End Firmware review.	Done	JC	19-12-02
Hold Electrical Test card review.	Done	JS	08-01-03

Actions outstanding and new actions		
Action	Who	Target Date
Produce FED software driver lib API.	JC	31-01-03
Organise lab space for FED tests.	RH/JC	17-01-03
Implement basic test firmware & test Chip Scope tools.	EF	17-01-03
Prepare loop back test for JTAG..	ST/RM	21-01-03
Release updated designs for BE & VME Firmware	RH	24-01-03
Arrange for Matt Noy to work part time at RAL	JC	24-01-03
Layout electrical test card (cross-point switch card)	DB	31-01-03

Project Monitor Form- milestones

Project: CMS FED		PMF number: 23		
Project Manager: J. Coughlan				
Date: Wednesday-15-January-2003		Sheet: 2 of 2		
	Milestones from Project Management Plan Version:1.3	date due in PMP	predicted date	date done
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off & PCB Tape Out	07.10.02	11.12.02	06.12.02
17	Batch 0 (2 off) Non-Opto Assembled boards at RAL	11.11.02	24.01.03	
18	OptoRx for Batch 0 in UK	26.08.02	06.01.03	
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	Batch 1 (10 off) Assembled boards at RAL	04.07.03		
22	Delivery Batch 1 to CERN start	12.09.03		
23	Delivery Batch 1 to CERN completed.	04.12.03		