Project Monitor Form

Project: CMS FED **Date:** Thursday 14-March-2002	**PMF number: 12** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

Customer has decided there is no advantage in producing a demo pcb with the FE Module analogue circuit. They have expressed concern about delay in analogue circuit design (approx 4 weeks wrt schedule.)

Manufacture:
Need to confirm availability of 2M/3M and place orders for FE FPGA in few days.

Front End Module:
James has proposed a modified analogue circuit. This requires an additional opamp on each channel to obtain VREF. He is now identifying a suitable component. He has produced an internal memo describing modification.
He also suggests using a DAC to derive common reference voltage for FE module (should be cheaper and more flexible solution.)

CERN have sent us final OptoRx pinout arrangement. This has accepted changes suggested by Adam and been OK'ed by him. There are still some uncertainties on method of heat dissipation from the module which will be clarified between CERN and company soon.

Whilst James is finalising analogue circuitry Chris is concentrating on digital layout. He has entered delay FPGA in library.

Firmware:
Delay FPGA:
Ed has passed details of final pinout and associated passives to Chris.
Ed has now tested both data phases of DDR outputs successfully and is making quantitative measurements of clock phase adjustment with DCMs.
He has 2 designs. One for engineering sample (still to be fitted on evaluation board) and one for commercial version. Difference is in DCM reset procedure. Choice of CES vs C has no effect on FE layout.

Board level:
Saeed has refined his table of power requirements and matched them to the LHC crate spec supplies. Conclusion is that it should be possible to derive additional supplies eg –5V, 1.5V on board. It was agreed to run ADCs on 3.3V (this is already done on H1 FTT.) QDRAMs require 2.5V from linear regulator. He has identified suitable switchers.
12 layer board would have 4 power + 8 signal planes, although it may be possible to manage with 10 layers (4 + 6).
When the updated Xilinx tools are available (in 2 weeks?) the FPGA power consumption figures will be recalculated for VirtexII.

Saeed has also (after discussion with Richard M.) proposed a scheme for JTAG test and configuration chains. This would involve 3 chains per board. He is investigating with Rob the

viability of a couple of alternative schemes.

Other Issues:

Actions from the previous PMF			
Action	**Status**	**Who**	**Target date**
Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	In progress	EF	31-02-02
Produce pinout of Delay FPGA for inspection by Adam.	Done	EF	
Make request to R. Stephenson to borrow simulations tools license for James's PC.	No need. James can use tools from Marcus.	RH	
Produce 1st order FE module analogue component layout.	Opamp section to be modified by James. Remainder ongoing.	CD/JS	25-02-02
Find out from Paul Hardy whether it is possible, and if so how, to automatically generate Xilinx FPGA symbols in CADENCE.	In progress.	RH/CD	25-02-02
Propose FED power distribution scheme following standard LHC crate PS specifications.	Done.	ST	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	EF	18-03-02
Verify fit of final design on evaluation board.	EF	25-03-02
Produce user manual for Delay chip.	EF	30-04-02
Pass updated analogue circuit to Chris.	JS	25-03-02
Update FE module analogue layout.	CD	15-04-02
Find out from Paul Hardy whether it is possible, and if so how, to automatically generate Xilinx FPGA symbols in CADENCE.	RH/CD	18-03-02
Order FPGAs for batch 0.	JC	18-03-02
Finalise and document JTAG test and configuration chains.	ST	25-03-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 11**		
Project Manager: R. Halsall **Date:** Thursday 07-March-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.0**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	**Project Spec sign off**	**21-12-01**		**05-02-02**
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	11-03-02	
5	FE Module Feasibility Review	28-02-02	11-03-02	
7	**Board Level Feasibility Review**	**04-03-02**	**08-04-02**	
8	Delay FPGA Interim Review	31-01-02	04-03-02	
9	Front End FPGA Interim Review	31-01-02	04-03-02	
10	Back End FPGA Interim Review	31-01-02	25-03-02	
11	VME FPGA Feasibility Review	28-02-02	25-03-02	
12	Clock FPGA Feasibility Review	28-02-02	25-03-02	
13	Release Test Plan Document	22-02-02	08-04-02	
14	FE Module Final Review	30-04-02		
15	BE Board Final Review	10-05-02		
16	Full Board Design Final Review	31-05-02		
17	**IDR Customer Production sign off**	**10-06-02**		
18	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**26-07-02**		
19	OptoRx for Batch 0 at RAL	26-08-02		
20	**Batch 0 Opto Assembled boards at RAL**	**01-11-02**		
21	Batch 0 review	06-01-03		
22	**Batch 1 (8 off) Assembled boards at RAL**	**21-03-03**		
23	**Delivery Batch 1 to CERN completed.**	**11-07-03**		