Project Monitor Form

Project: CMS FED	**PMF number: 52**
Date: Friday 14 Jan-2005	**Sheet:** 1 **of** 2

Project Implementation phase.

FEDv2

Manufacture of Pre-series
Production of **5 + 20** off FEDv2:

Assembly of first 5 boards commenced week of Dec 13th as anticipated. However, there were problems discovered with the metal finish of the pcbs (gold not attaching to a number of pads). It was found that even after repair at DDi Tewskbury the boards were not acceptable for assembly. Therefore pcbs from the 2nd batch of 20, which are ok have been used instead. DDi will manufacture more pcbs to make up the difference, but this should not affect the overall schedule. There was one board which had the bottom side assembled before the metallisation problem was discovered. As we couldn't be fully confident that the top side is safe for BGA assembly it was decided not to attempt the top side assembly.

Otherwise the assembly went smoothly with only minor queries. We expect 5 boards to be delivered on Friday 14th Jan. Allowing 2 weeks for commissioning, the assembly of the remaining 20 boards will now commence week starting Mon 31st Dec. Assembled boards will be delivered in 4 batches of 5 commencing week of Mon Feb 21st.

Design Testing :

Tests on S-LINK readout on FEDv2 are continuing.
The BE FPGA timing has been adjusted and no S-LINK errors have been observed during high rate/occupancy runs of over 10^9 events.
VME readout may also need some adjusting, although tests of up to 10^7 events have reported no errors.

A preliminary report detailing the results of FE Analogue tests by Stefanos Dris at CERN of FEDv1 concluded that the load resistor should be lowered to 62 Ohm, but there is no improvement in settling time in changing the ADC input capacitor value from 4.7 pF.
Results need to be confirmed on a FEDv2.

Firmware :

TTC chan B commands : Resync has been implemented (needs testing).

Two new Tracker header formats have been introduced :
i) “Full Debug mode” with existing full status information from APVs and FE lengths plus an extra word containing mode and diagnostic information
ii) “APV Error mode” with condensed status information* on APV status and without FE lengths.
See latest BE FPGA technical description for full details at
http://www.te.rl.ac.uk/esdg/cms-fed/firmware/Documents/BE_FPGA_Technical_Description.doc

*The full debug information is also provided in VME registers for monitoring (needs testing).

Sufficient information is provided to enable the readout software to recognise header and reconstruct event information. Readout software will need updating to handle mode ii).

Assembly Plant Testing

The manufacture test plan procedures have been optimised and this is also implemented in the LabView application.

DDi test section chief Peter Stoneham visited RAL on 30 Nov to inspect our existing test set-up and procedures. They were very satisfied with the arrangements and do not envisage any difficulties in carrying out our proposals for test. It was decided that we would provide DDi with all the equipment (including Boundary Scan kit) needed for the Assembly plant testing.
This was followed up with a visit to DDi on 6th Jan to inspect the assembly plant and test facilities and for further discussions with Peter Stoneham.
JTAG representative James Stanbridge visited RAL 7th Dec and demonstrated improved Boundary Scan tools.

Other Items

Ivan modified (e.g. 62 Ohm resistors) 5 existing FEDv1 boards at CERN (nrs 005, 013, 014, 015, 016).
However, the proposed upgrade (by adding LVDS clock) to be compatible with latest FEDv2 firmware was not successful (due to bug in Firmware which is now corrected).
Nb |CFlash cards were then inadvertently reloaded with slightly out of date v1 firmware, but this should not affect LSA testing.
Recommended FEDv1 firmware is still:
ACE File: 16_07_04_1500 = (Delay 02_1B ; FE 03_16 ; BE 02_43)
EPROM : VME_03_0F
Two boards still report problems. Plan to send back to RAL for investigation.
Nr 17 at RAL is being modified and re-tested as a replacement.

The spreadsheet detailing the location and status of all FED boards has been updated on the web.

Final FED crate order has been submitted with clarification of crate specs after discussions with Paul Harwood at CERN ESS.

James and Greg successfully installed full 4 x FED Tester system at RAL with a FED Kit and the latest test software. Full speed readout tests are now being carried out at RAL.

Lab area at RAL has being rearranged in preparation for arrival of the rack from CERN.
Some kit needed for full crate tests is missing (e.g. second LHC crate, suitable crate controller). To be discussed at this meeting.

Final Production:

Updated quote from DDi, which adds assembly testing and front panel manufacture costs, has been received.

Our submission to the CERN Finance Committee in March has been correspondingly revised.

A full stock check of components remaining at RAL after pre-series production is in progress. Components on long lead times are being identified in collaboration with DDi with a view to RAL purchasing sufficient quantities to avoid delays in starting the first batch of the final production (DDi can't commence procurement until a contract is agreed).

A follow up meeting with DDi to discuss contract issues is proposed for end of Feb.