Project Monitor Form

Project: CMS FED **Date:** Monday 14-January-2002	**PMF number: 04** **Sheet:** 1 **of** 2

News and comment
Feasibility Study continues.

Planning:
Following last Thursday's customer meeting version 1.0 of the Project Schedule and a draft v 0.1 Project Spec have been released to them.

Front End Module:
Despite considerable effort on our part the problems using AWB and the current CADENCE releases is still not resolved. In order for Chris to proceed with the overview and layout James and Adam will provide schematics of the FE module in paper form starting with H1 basic design with annotations for CMS specific components.
Chris also requested information on the specs for the VME board. It is intended to follow the VME 64x standards.
It was noted that the Mezzanine CMC card now holding the electrical DAQ link provided by the CERN group is no longer on the FED motherboard (only original opto link was feasible on the motherboard). It seems likely that we will need to provide VME Transition cards to hold CMCs (one per FED). In the short term this could be implemented as part of the JTAG loop back test card for the Prototype FEDs.
The urgent need to start the FED board level design was noted.

Firmware:
Ed is continuing tests of the DCM using the Virtex II 40K evaluation board. Using a simplified design the output clock is now observed but does not yet respond to the phase shift commands.

Rob and Saeed met with Azmat last week to review the status of the BE FPGA and handover the design libraries and existing documentation.

Actions from the previous PMF

Action	Status	Who	Target date
Approve draft Project Spec & FED prototype costings before customer meeting.	Done	JC	
Develop draft schedule	Done	JC	
Produce procurement list for 9U Prototype	Ongoing	RH	17-12-01
Check Impact Memec if Cadence Xilinx footprints/symbols exist on Xilinx Web site	Ongoing	RH	
Organise a Board Level Design Meeting	Done	RH	
Organise hand over meeting for Back End FPGA	Done	RH	

Pass schematic for Analogue part of Front End module to DO	In progress	JS/CD	17-01-02
Test key aspect of Delay FPGA on development board in Lab	In progress	EF/RH	31-01-02

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Produce procurement list for 9U Prototype	JC	31-01-02
Check Impact Memec if Cadence Xilinx footprints/symbols exist on Xilinx Web site	RH	21-01-02
Pass schematic for Analogue part of Front End module to DO	JS/CD	21-01-02
Test key aspect of Delay FPGA on development board in Lab	EF/RH	31-01-02
Send Chris pinout of OptoReceiver	JC	21-01-02
Send Chris VME specs	RH	21-01-02
Change access privileges on CMS-FED Projects area	RH	21-01-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 04**		
Project Manager: R. Halsall **Date:** Monday 14-January-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01	31-01-02	
3	Board Level Preliminary Review	14-01-02	14-01-02	
4	FE Analogue Channel Feasibility Review	31-01-02	31-01-02	
5	FE Module Feasibility Review	28-02-02	28-02-02	
7	Board Level Feasibility Review	04-03-02	04-03-02	
8	Delay FPGA Feasibility Review	31-01-02	31-01-02	
9	Front End FPGA Feasibility Review	31-01-02	31-01-02	
10	Back End FPGA Feasibility Review	31-01-02	31-01-02	
11	VME FPGA Feasibility Review	28-02-02	28-02-02	
12	Clock FPGA Feasibility Review	28-02-02	28-02-02	
13	Release Test Plan Document	22-02-02	22-02-02	