Project Monitor Form

Project: CMS FED **Date:** Friday 13-December-2002	**PMF number: 22** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment
Regular Project Monitor Forms will now serve as Reports for FED-UK meetings.

Schedule:

We have so far kept to "day by day" task schedule (see spreadsheet) presented at last FED-UK meeting 31.11.02. We have maintained regular reports on progress to IC.
Major effort from Drawing office.

PCB files went out Friday 6th Dec. Expecting 2 PCBs back by Friday.
(Remaining 4 in 15 working days).
Prices were encouraging. Tooling charges also waived.

Additional files required by Assembly company should be completed on Friday. We can then obtain quotes.

On schedule planned boards & kit out to Assembly company on Wednesday 18th.
If we shipped out on Monday 16th and everything went well it is still possible we could get assembled boards before Xmas shutdown.

It is unlikely any test work would start before Week 2.

The major concern now is availability of replacement XC2V40 FPGAs (see Procurement Propose to ship FEDv1 kit except for XC2V40 so that rest can be checked. Then send on replacements when they arrive).
Question: How long can we wait for replacements?

Procurement:

Problem: XC2V40 Delay FPGAs.
Xilinx distributor IMPACT Memec visited 11th Dec.
Existing parts are confirmed as Engineering Samples.
They are unable to obtain more details from Xilinx.
Replacements would only come with our existing order for next 20 FEDs.
(XC2V40s were on longest,12 week, leadtimes. All other FPGAs from that order have arrived).
Replacements have left US. Still awaiting likely ETA at RAL from Impact. They were confident that they would be there by Jan week 2.

We agreed to make a request (under Xilinx NDA) for a 12 month price FPGA forecast to get a better prediction of production costs.

Testing:

Rolling Day by Day task schedule needs to include testing next.

Bare board visual checking of PCB and tests for shorts when they arrive.

Ready to assemble VME crate at RAL next week, once backplane arrives.
Would like extender card for JTAG tests.

Design of the Electrical test board (using .Cross point switch plus AD8131 Opamps) is complete.
Awaiting Cross-point component to be entered into Cadence library by Drawing office. After that schematics can be reviewed and the job passed to Drawing Office. (Depends on Drawing office effort availability).

Test Lab consider that JTAG testing of FEDv1 connectors requires a loop back pcb to be designed and made. We need to verify if we can make do with extender card for first board tests as planned. Need pcb for larger production runs.

PPD are working on temp control for Opto Test card. Not part of FED spec.
Requires loan of NI/PCI-VME interface. Some assistance with software installation may be required.
PC for DAQ-LINK testing has been ordered by PPD. It has 4 independent PCI-X slots. NB NI/MXI PCI-VME interface card uses 5V buffer logic and will not work in this PC.

Firmware:

VME-FPGA:
Use of Block Ram resources has been reduced. Engine reading serial stream from FE FPGAs (via BE FPGA) is almost working.

BE FPGA
Improved data path to and from QDR Memories is implemented.
Clock section completed.
List of remaining tasks exists and to be reviewed.

Ready now for a review of the BackEnd and VME Firmware. (it had to be postponed this week due to illness).

Software:
Succeeded in installing Laurent Mirabito's Tracker DAQ packages.
Installed and tested FED-PMC drivers.
Installed and verified simple memory access using NI/VXI VME interface drivers under Linux.

Effort:
Test Engineer Ivan Church was requested at 30% in December. We have not been able obtain a significant fraction of his time as yet.

CMS News:
30 tested OptoRx will be available by end of December.

A document describing the module tester functionality requirements in 2003 of FEDv1 has been received from CERN. There don't appear to be any major surprises. A reply has been drafted. To be discussed at FED-UK meeting 13.12.02.

A shortage of FED-PMCs for CMS has been reported by CERN.
Plan proposed to see what we can do about it. See accompanying slides.

AOB:

FED web area is in process of re-organisation. Apologies for any inconvenience.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
FED board ready for internal Design Office check	Done.	CD	
Tape out to PCB manufacture.	Done on 06-12-02.	CD	
Produce FED software driver lib API.		JC	29-11-02
Order DAQ PC.	Done	IT	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Produce FED software driver lib API.	JC	31-01-03
Complete Assembly drawings.	CD	13-12-02
Get FED Kit ready for Assembly company.	BT	18-12-02
Store copies of FED schematics, drawings etc on project web.	JC	20-12-02
Assemble VME crate.	IC	20-12-02
Hold Back-End Firmware review.	JC	10-01-03
Produce Electrical Test card schematics.	JS	18-12-02
Hold Electrical Test card review.	JC	20-12-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 22**		
Project Manager: J. Coughlan **Date:** Friday-13-December-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02	20.12.02	
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off&Board Out**	**07.10.02**	**11.12.02**	**06.12.02**
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**	**24.01.03**	
18	OptoRx for Batch 0 in UK	26.08.02	06.01.03	
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		