Project Monitor Form

Project: CMS FED **Date:** Tuesday 13 March-2007	**PMF number: 66** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

No further deliveries to CERN since last PMF.
Full details in Production spreadsheet.

FEDs

The long awaited move of the electronics lab with CMS rack from R25 to R12 took place week of March 5th. The moved system will be reconnected when Ivan is back from CERN next week. There is a new cooling unit in R12.
Some of the remaining 16 good boards may require final overnight test.

We are experiencing long delays and poor response from Exception for the repairs to final 10 boards.

One board tripping with Over Temp. Discovered ORx pull up values wrong. Now fixed. Checked nr of other boards were ok.

A final batch of 40 ORx will be available from NGK Japan in April 2008 (once the guarantee period is over and assuming no claims have been made). A further 40 ORx will be recovered from test systems. This should allow us eventually to equip the remaining ~ 10 unpopulated FEDs. Plan is to fit ORx at RAL.

CERN Contract

Payment of final invoice has been received from CERN.
After final payment Project code RQ09600 is left with positive balance of £24,735

CERN USC Installation and Commissioning :

With assistance from Ivan a total of 5 more Tracker FED crates were installed in rack S1B03 and S1B05 in USC55.
A total of 8 USC crates have now been populated with FEDs.
DAQ group have tested FRL and FMM links.
DAQ group plan to do a full partition test next.
For latest news see ELOG http://tacweb.cern.ch:8080/elog/Cessy-VME/

A rack grounding scheme is being implemented to eliminate noise seen on FMM links (noise observed even though these are LVDS signals).

SLINK Transition Cards

Agreed to return first batch of ~ 70 cards from CERN (with unshielded RJ45 connectors). Ivan to arrange for shielded connectors to be fitted by Cemgraft. They are difficult to fit without proper equipment. (see last PMF for details).

Firmware and System Integration Tests

Outstanding issues.

1. Module readout tests at CERN have recently discovered a trigger rate related noise on the wings of the APVs (at APV edges). The effect only starts to increase around L1 50kHz and increases with rate.
In order to investigate pedestals readout of raw data at these rates is needed. The highest rate achieved with 100MB/s readout over Slink and all FEUnits disabled but one, is 15kHz. Disabling individual Disabling channels to speed readout does not work…
Tests (using nice Fake data)

- Setting 'Load Tick Command' aka APV disable.
It looks like Bill interpreted disabling channels as not using them in Header majority detection logic. But he always reads out all 12 fibres. The disabled channels are flagged in the header so that the data can be "disabled/removed" offline.
Unless you disable all 12 which kills all readout from this FPGA. So all or nothing.

- Setting 'Load Thresh Command' to max to disable frame finding on that fibre.
Again the fibres for which no frames are seen are flagged in event header for offline removal. But all 12 fibres are still read out.

This behaviour is entirely consistent with Bill's Technical description.
Disabling the actual readout of individual fibres is probably quite difficult to do in the logic.
Not yet convinced that it is really necessary in normal operations.

Instead have implemented down scaling on Frame capture on FE (Tick master logic) and correspondingly in BE to keep frame and trigger synchronization.
Awaiting results from CERN.

2. Channel B tests. APVe pipeline broadcast to FEDs via TTC (already tested at RAL).
Initial tests at CERN were confused by software not enabling serial B output on TTCrx. Propose to initialize TTCrx internal control register to enable chan B serial output at FED power on (as per LM82 threshold values).
Jon now verifies APVe values are in FED headers. We verified that long commands received from TTC have APVe data words in correct format.

3. Event Format changes to improve Filter unpacking efficiency. Necessary changes to BE have been investigated. Propose to implement and test at RAL first.

4. New DELAY FPGA Spy channel with synchronous frame capture tested at CERN. New Imperial student is going to provide software to unpack data.

5. DELAY FPGA Fine Skew (versions …24 and later). Should improve timing calibration. But it has not yet been verified at CERN.

Misc Problems…

6. There is a problem with ZS Lite event readout for events which have no hits? Standard ZS readout is ok.
This seems to be an initialization issue. Repeat initialization and don't see problems.
Suggestion from Saeed that it could be due to control register setup in FE FPGA?

7. DAQ column (TOB tests?) problems with spurious events at start of run are still observed.

8. Problems when software reloading from SYSTEM ACE CF seen at CERN (Delay FPGAs fail to load). Several suggestions made for further investigation. No further news from CERN.

9. Board in USC55 with stuck VME bits?

Update on the earlier modifications..

```
2. Add 8 FE Full Flags to the register in the Special Tracker Header. This
register would indicate that any one FE FPGA buffer has entered the overflow
condition. This needs to be investigated in order to find out how best to use
it to indicate the payload data is corrupt/overwritten. I will try to discuss
with Oz re best way to implement.
RELEASED and TESTED at CERN.

3. Change BE Status Register Two from 64 bits to 32 bits (already discussed
with JF and Jo).
RELEASED and TESTED at CERN.

4. Does JF require a reset sent to the ACE System after a vme reset is
issued? At the moment this is not happening. Need to discuss with JF. This is
to do with problems reading DLY FPGA after an ACE file upload.
NO LONGER REQUIRED

5. Remove TTC_Ready signal from the BE Command Decoder, as this is redundant.
TBD

6. Store the two software DAQ registers in the Tracker Headers in a FIFO at
the time L1A is received (requested by JF).
This is the most complex mod at this stage of development. Therefore all
other mods must be checked to ensure no errors are introduced in the BE f/w
before this change is made.
RELEASED and TESTED at CERN.
```

Consider using ELOG system for FED firmware problem reporting.

Tracker Electronic Systems meeting at CERN today (by VRVS).

FED slides presented.

Request from Geoff to send 16 good FEDs to CERN.

Slawek would like procedures to manage releases of FED firmware. Needs automated system?
Laurent proposes following validation of new firmware in 904 that it is installed on all FEDs at TIF and tested on Monday morning (during system test period).

Request to CERN personnel to add ELOG to record FED related problems.

Slawek would like some form of regression test of ZS at each new release.
Slawek suggests meeting dedicated to ZS algorithm. There are indications from unreleased studies that comparisons of ZS and Raw Data give incompatible results. NB Register level operation can only be absolutely tested with Spy channel.

Documentation

Draft of updated Delay FPGA Technical document was released. Describes new Spy channel. Awaiting comments from Jo.

VME FPGA Technical document is also being updated. Needs major rewrite.

sLHC

Meeting was held at Imperial on 16th Jan to discuss possible work packages for a Tracker upgrade UK bid in June. Including new APV and FED.
Follow up meeting later this week.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Test BLT for System ACE CF loading		JC	01-11-06
Fix Synchronisation problems seen in MTCC	Waiting TOB results.	ST	01-11-06
Test CF reloading with old ACE files, resistor terminations	Awaiting results.	OZ	01-04-07
Suggest shielding scheme on Transition card.	Done	IC	
Decide on event format proposal.	Done. Will do it.	JC	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Test BLT for System ACE CF loading	JC	01-04-07
Test CF reloading with old ACE files, resistor terminations	OZ	01-04-07
Find out what has happened to boards under repair at Exception	JC	16-03-07
Provide draft of work package for FED SLHC upgrade	JC	16-03-07
Implement new Event Format and Test with memory dump	ST	30-03-07
Update fedDebug program to process new Event Format	JC	30-03-07
Send 16 good FEDs to CERN	IC	30-03-07

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 66**		
Project Manager: J. Coughlan **Date:** Tuesday 13 March-2007		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05		28.07.05
33	Production of 500 FEDv3 starts	08.09.05		01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05		27.10.05
35	First FED installed at USC55	17.11.05		19.10.06
36	Last FED installed at USC55	26.07.06	01.06.07	
37	Power on Tracker at USC55	01.08.06	01.07.07	
38	Readout test with Tracker at USC55	01.10.06	01.08.07	
39	LHC test run	02.04.07	01.11.07	