Project Monitor Form

Project: CMS FED **Date:** Friday 12 September-2003	**PMF number: 36** **Sheet:** 1 **of** 2

Project Implementation phase.

FEDv1:

Manufacture

6 FEDv1 bare PCBs (Tin finish) arrived on 5th September.
Went out for assembly (with all Optos) on 9th September. With explicit list of those components on schematics not to fit.

Ser 005 (with 8 Optos) has been tested. Readout of empty events tested. Brought to Imperial today for optical testing.
NB Requires a different Cflash file due to XC2V1500 FE FPGA parts. Actual FPGA firmware should be IDENTICAL.

Got updated set of Xilinx quotes (now from Unique Memec.)
These figures should reflect close to our final pricing for final volumes.
It looks encouraging. All target parts are close to our estimates of 50% of first quotes.
It would be interesting to compare what prices CERN could achieve?

Analogue Devices (eg ADCs) are now distributed by AVNET. Although the contact person has just moved from MEMEC.

Internal Interim Review of FED status held on 11th September. Status of FEDv1 and possible changes to FEDv2 design reviewed.
The full list of changes implemented for the CALICE version of card will be introduced on FEDv2.

Order of 25 off TrueLight pin diodes for TTCrx arrived from Taiwan.

James Salisbury has commenced work on another project. Work on power circuitry was handed over to Ivan. James is still available for assistance is needed (e.g. investigating analogue effects.)

Bigger power supply was installed in main 9U crate. A second 9U crate (with fewer slots) will be adapted for future power testing.

Firmware

FE-FPGA:

Finding problem with empty data on some channels. Now suspect firmware handling DDR input data (was changed to solve an earlier problem.) Under investigation.
But some software that allows us to see the data graphically would help a lot.
Frame Finding is starting to work at Imperial using OptoTest card inputs.

BE FPGA:

Verified readout with back plane LVDS clock and trigger using SEQSI.

Tests with TTCrx:
I2C interface for setting up TTCrx registers (clock delays etc..) (adapted mostly from borrowed Atlas code) was implemented and appears to be working (version BE 02_1D.)
Need to set all jumpers on TTCrx pins to set up I2C address etc.

This interface will be further adapted for controlling LM82 Temp sensor (makes setting up via software a lot easier, it has never worked yet!)

We have not been able to get a stable 40 MHz clock out of TTCrx. Now suspect that our TTCvi is not programmed correctly (or even faulty?).
Have checked TTC on both 002 and 005.
Verified that normally TTCrx is receiving the appropriate reset signal (although in our crate sometimes the power cycle pin needs holding down for a couple of seconds to ensure this.)

Next step is to check TTCvi/ex against cards at Imperial and in Atlas PPD.

VME FPGA:
We can now handle “big” events that fill more than a single VME buffer (32 Kbytes) as needed for Frame Finding with all 96 channels.
Stable version is VME 01_F5

Block Transfer event readout verified (over NI/MXI.)

Now adding a status register to indicate serial commands have completed.

Basic functions for LSA are now in place.

Ed Freeman is going on to other projects at the end of this month. He will be available to help us if necessary.
Saeed will take over responsibility for design.

DELAY FPGA:
Before he leaves us Ed will look at fine adjustment of clock skew settings to iron our jumps.
Saeed will take over maintenance of design, but don’t expect any major changes needed.

<u>Other Work</u>

S-LINK:
We now have ECAL Transition card for S-LINK PMC tests. Needs some mods before we can use it.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Get 2nd VME64x test crate operational	Backplane just arrived	IC	19-09-03
Get TTCrx clock output working.	Need to verify TTCvi/ex cards	ST/JC	12-09-03
Get Multi-Fragment Events readout in VME	Done	EF/JC	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Get TTCrx clock output working.	ST/JC	19-09-03
Get 2nd VME64x test crate operational	IC	26-09-03
Fix problem in FE FPGA input data	IC/JC	19-09-03
Contact RAL Contracts re FED tendering	JC	19-09-03

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 36**		
Project Manager: J. Coughlan **Date:** Friday 12-September-2003		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off &PCB Tape Out**	**07.10.02**		**06.12.02**
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**		**22.01.03**
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		